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ACOUSTICALLY SCANNED OPTICAL IMAGING DEVICES

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1 July — 31 December 1977

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February 1978

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have been made.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)
We have made the first successful ZnO on Si storage correlator and have correlated signals with a time-bandwidth product of 30,000. We have constructed a GaAs convolver with good results, and are in the process of making a GaAs correlator. Complete theory of the storage correlator has been developed and checks well with experiments.
have been constructed
have been correlated

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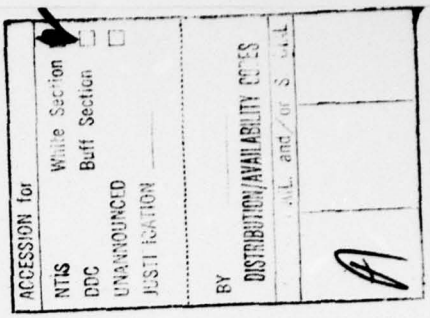

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MANAGEMENT REPORT

As anticipated, the major problem encountered since the start of the new program in October is with a supply of GaAs. We do not, however, anticipate that this will hold us up. Originally we had expected to obtain this material from Teledyne MEC. It was to be grown there by Bob Adams who has considerable expertise in the field. He has already supplied us with four slices from Teledyne MEC, enough for our needs until the end of February. However, he left Teledyne MEC a few months ago.

Since that time, we have had considerable contact with Adams and his co-workers at Motorola in Arizona. They have promised to supply us with the material we need and appear to be making good progress in this direction. All the contacts so far with Adams have been encouraging, and there do not appear to be any hitches.

In addition we have been supplied by R. Moon at Varian Associates with material of the type we require, although the individual slices are rather small for our needs. The carrier density and quality of the material is in the correct range. They should supply us with more material of larger size within the next week.

A further source of supply whom we have contacted is Standard Telephone Laboratories in England. They are themsleves interested in making surface wave correlators out of GaAs. So, in exchange for help with the design of the correlators, they are willing to supply us with GaAs. At the present time the quality and size of their material is not adequate, but they will be developing their technology, and they would expect to be able to send us material within the next one or two months.

We therefore feel that our source of GaAs supply is sufficiently well-assured that we can continue this program with confidence.

We should add that there is also a Japanese commercial source from whom we may be able to buy this material; but the price is extremely high, and the minimum amounts they wish to supply are too large for our needs. If all else fails, we will pursue this possible source further.

At the time of writing, which is approximately one month after the end of the period covered by this progress report, we have made our first monolithic GaAs convolver. It has worked extremely satisfactorily with far better performance than we had anticipated for our first try. The device has not been constructed as a correlator only a convolver. Because of the extremely encouraging results, we intend to go on and build a correlator directly without an initial careful investigation of the technology, as the difficulties do not seem to have been as severe as we had anticipated.

FISCAL STATUS

Total amount of contract	$504,302
Expenditures & commitments through 12/31/77	$227,424
Estimated funds required to complete work	$276,878
Estimated date of completion of work	30 September 1980

During this period a Hewlett Packard 1740A 275 MHz oscilloscope was purchased at a cost of $2100. This oscilloscope should prove helpful in measuring rf and pulse waveforms directly.

I. SUMMARY

During the last six months considerable progress has been made on both our ZnO on Si devices, our development of GaAs devices, and our theory and experiments on air gap devices. Several papers have been published and given orally at the Ultrasonics Symposium. These papers are enclosed as Appendices to the report and give a fairly good summary of our work up to last November. In addition, a thesis on the air gap correlator with a detailed theory of its performance is in the process of being written. The chapter of this thesis on the analytic theory of the diode storage correlator is enclosed as an Appendix in its entirety, because we believe that this theory is of major importance. For the first time it gives a detailed quantitative picture of the operation of the storage correlator and agrees in all respects but one minor one concerning the charging time of p-n diodes with our experiments and those of others. During the last few months we have been covering this aspect of charging time of p-n diodes and have managed to satisfy ourselves as to where the difficulties have lain. An outline of the theory, carried out by Tuan on the subject, is also given in this report.

Experimentally we have constructed both air gap and ZnO on Si storage correlators and correlated FM chirps, Barker codes, and so on. A major breakthrough has been to demonstrate that we can correlate codes with a time-bandwidth product as large as 30,000 in a storage correlator. This should prove extremely useful in its application to spread spectrum communications as well as radar systems.

Both on this contract and others we have been carrying out analyses of the operation of inverse filters and equalizers. We believe that the

storage correlator is ideally suited to the construction of adaptive filters which could correct errors due to atmospheric turbulance, to communication systems themselves, and so on. On other contracts we have carried out demonstrations of transversal filters which are controlled by a microprocessor although they are operated at relatively low frequencies. In one case, we used a CCD tapped delay line. We are also carrying out direct computations using a signal read into a computer and correcting errors in it by adaptive processing. This is giving us considerable experience in the algorithms necessary for the process.

The ZnO on Si correlator has made good progress. We now appear to be able to deposit ZnO reliably although slowly and have constructed some good working devices. The results are summarized both in the body of this report and in the enclosed papers. Some difficulties have been encountered with the silicon technology associated with the devices, evidently because the surface states in the silicon can be effected by the deposition of ZnO. Thus, some of the devices we have constructed did not operate satisfactorily, although previous ones had. We anticipate that this is a minor difficulty which will be solved on later runs. But it does point out how convenient it is to work with GaAs which does not have these difficulties because no ZnO is deposited on the active region.

During the course of our work on GaAs, we observed certain defects caused by alloying of gold with the GaAs under special conditions. It turned out that we could examine these defects, which were not visible optically on the top surfaces of the gold, very conveniently with the acoustic microscope. So some time was spent with the group under

Dr. Quate looking at these kinds of defects by this technique. We believe the technique is a very powerful one, and it proved very useful in this case. However, unfortunately from the point of view of proving the efficacy of the acoustic microscope in our experiments, this type of defect proved to be very rare. Nevertheless, it does point out that there are certain features which are extremely difficult to detect by other techniques unless the gold is first removed but which show up very clearly with the acoustic microscope, even though these defects were in the GaAs under the gold layers.

At the time of writing, which is approximately one month after the end of the period covered by this progress report, we have made our first monolithic GaAs convolver. It has worked extremely satisfactorily with far better performance than we had anticipated for our first try. The device has not been constructed as a correlator only a convolver. Because of the extremely encouraging results, we intend to go on and build a correlator directly without an initial careful investigation of the technology, as the difficulties do not seem to have been as severe as we had anticipated.

LIST OF PAPERS PRESENTED AND PUBLISHED DURING THIS PERIOD

P.G. Borden and G.S. Kino, "An Analytic Theory for the Storage Correlator," presented at the 1977 IEEE Ultrasonics Symposium.

H.C. Tuan, B.T. Khuri-Yakub, and G.S. Kino, "A New Zinc-Oxide-on-Silicon Monolithic Storage Correlator," Presented at the 1977 IEEE Ultrasonics Symposium.

P. Borden and G.S. Kino, "Input Correlation with the ASW Storage Correlator," Published in Electronics Letters 13, #16, 470-471 (4 August 1977).

P. Borden and G.S. Kino, "The Charging Process in the Acoustic Surface Wave p-n Diode Storage Correlator," Published in Applied Physics Letters 31, #8, 488-490 (15 October 1977).

H.C. Tuan and G.S. Kino, "A Monolithic Zinc-Oxide-on-Silicon p-n-Diode Storage Correlator," Published in Applied Physics Letters 31, #10, 641-643 (15 November 1977).

H.C. Tuan and G.S. Kino, "Large-Time-Bandwidth-Product Correlation and Holographic Storage with an SAW Storage Correlator," Published in Electronics Letters 13, #24, 709-710 (24 November 1977).

II. PROGRESS ON GaAs CORRELATOR TECHNOLOGY

Significant progress has been made in the fabrication of Schottky and ohmic contacts. We have found that the final step in the predeposition cleaning process is the most critical. We have also found that it is important not only to remove all oxides, but also to minimize the formation of new oxides between the cleaning and deposition steps. By using a final step of 1:1 HCl:Methanol followed by rinsing in Methanol with minimum exposure to air during sample loading, we have increased the breakdown voltages to values which are consistently over 100 V. The reverse currents have also been reduced to less than 10^{-7} A cm^2 for a diode of area 3 mm^2. The electrical characteristics of the Au or Al diodes do not change with heating to 300°C in vacuum. We have considered trying more sophisticated multilayer Schottky diodes; however, because of mass loading of the surface, a monolithic storage correlator is adversely affected by thick metallizations.

Ohmic contacts for the backside ground contact have been made using a 4000 Å thick layer of eutectic Ge-Au. The layer was annealed at 500°C in forming gas for 2 minutes. This was found to be the minimum time necessary to get relatively low contact resistance (30 Ω-cm^2). Balling up of the Ge-Au film has not proved to be a significant problem.

Previous storage correlators made at Stanford used a wavelength of 32 microns. We intend to fabricate correlators which operate at a wavelength of 16 microns (160 MHz). New masks for transducers and diode arrays have been designed and tested. The diode array contains diodes of 3 micron width with 3 micron spacing. A pattern of some aluminum

diodes is shown in Fig. 1. These dimensions are smaller than have previously been obtained at Stanford's integrated circuits laboratory using conventional photolithography.

We have made a number of airgap diode convolvers using gold Schottky barrier diodes without oxide between the diodes. The convolution efficiency was -80 to -82 dBm. External dc biases of + 500 V to - 500 V affect the output by less than 3 dB. The low convolution efficiency thus appears to at least partly be due to a high surface state density. Subsequently, native oxide was grown between the diodes. A solution of potassium permanganate dissolved in acetone was used in one case, and a solution of sodium phosphate dissolved in water in the other case. The permanganate solution attacked the gold diodes. The convolution efficiency was improved by 2 dB when the second solution was used. We shall attempt to obtain much greater improvement by first growing the oxide and then depositing the gold layer. We are also investigating the effects of sputtered and pyrolytic oxides.

Two studies have been initiated in conjunction with Prof Gibbons' ion implantation group at Stanford. We are making a p^+/n diode correlator using implanted zinc ions. The implantation has been done, and a cap of 1000 Å silicon nitride and 7000 Å SiO_2 has been deposited on the sample. The diode array will be annealed at 800°C for 30 minutes. We are also investigating the effects of proton bombardment on reducing the leakage current between diodes. The initial results are encouraging.

We intend to use ZnO on Au films under the transducers of the storage correlator to increase the piezoelectric coupling. We have found the optimum parameters for the gold deposition and are investigating the optimum parameters for the ZnO deposition.

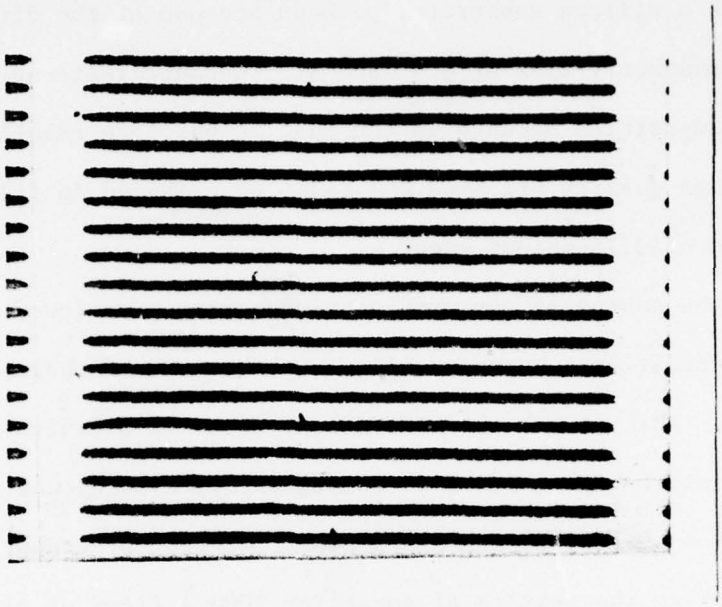


FIG. 1--Aℓ Schottky diodes on GaAs. 800×.

The optimum deposition conditions are slightly different from the case with a silicon substrate, perhaps because of the difference in the thermal conductivities of GaAs and Si. We anticipate no problems with the ZnO deposition because in the past it has been relatively easy to obtain high quality oriented ZnO films on oriented Au films when a substrate of silicon was used.

In the course of our work on diode arrays, we found that under certain conditions, apparent alloying behavior was observed optically (Fig. 2). This effect was much more evident in pictures taken using an acoustic microscope (Fig. 3). Consequently, a study was initiated in conjunction with Prof. Quate's acoustic microscopy group. We are investigating the results of annealing 1000 $\mathring{A}$ films of Al, Ni, Au and Ti (50 $\mathring{A}$) Au. Acoustic and optical pictures of a Au on GaAs sample before annealing are shown in Fig. 4. Pictures of the same area after annealing at 175^{o}C and 275^{o}C in vacuum are shown in Figs. 5 and 6. Pictures of a different Au on GaAs sample that was annealed at 400^{o}C in vacuum are shown in Fig. 7. In this case the effects of the anneal are very evident in both the optical and acoustic pictures. We are also conducting a series of anneals at atmospheric pressure. Verification of alloying behavior such as that indicated in Fig. 3 will be done through SIMS measurements. We hope to be able to detect acoustically the shape and size of alloying that has been referred to in the literature (from Auger measurements) as nonuniform alloying. This may demonstrate an important new use for the acoustic microscope.

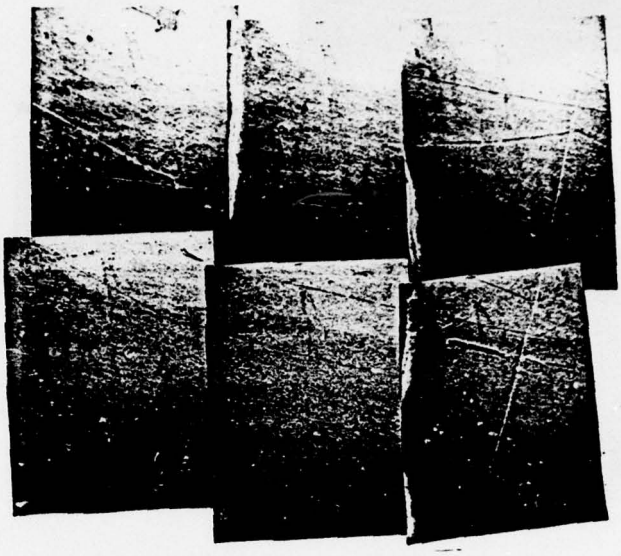


FIG. 2--Optical picture of Au on GaAs after annealing. 300×.

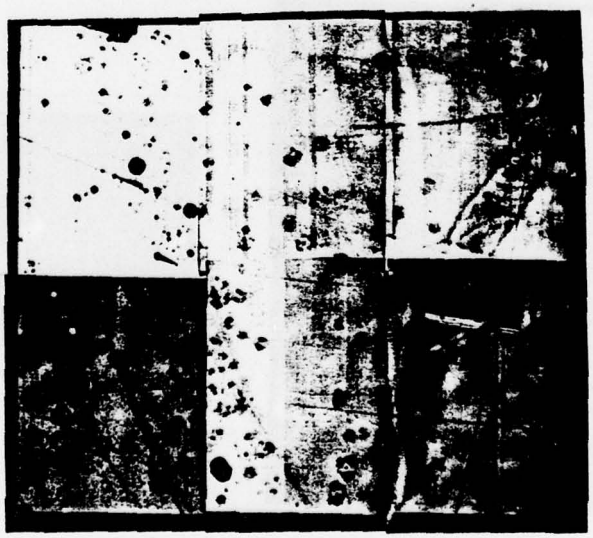


FIG. 3--Acoustic picture of Au on GaAs after annealing. 300×.

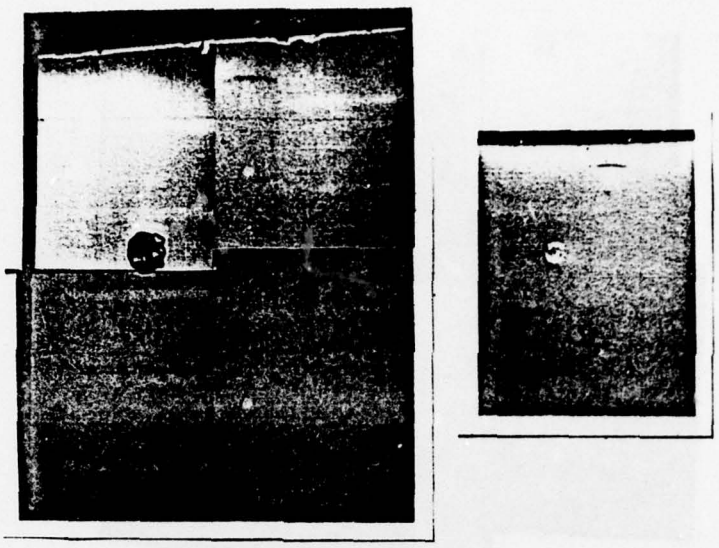


FIG. 4--Pictures of Au on GaAs before annealing.
(a) Acoustic 300×;
(b) Optical 150×.

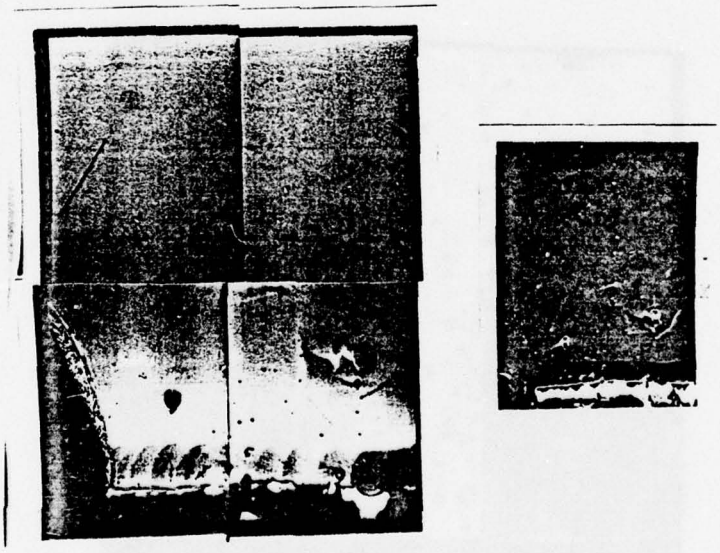


FIG. 5--Pictures of Au on GaAs after annealing at 175°C.
(a) Acoustic 300× ;
(b) Optical 150× .

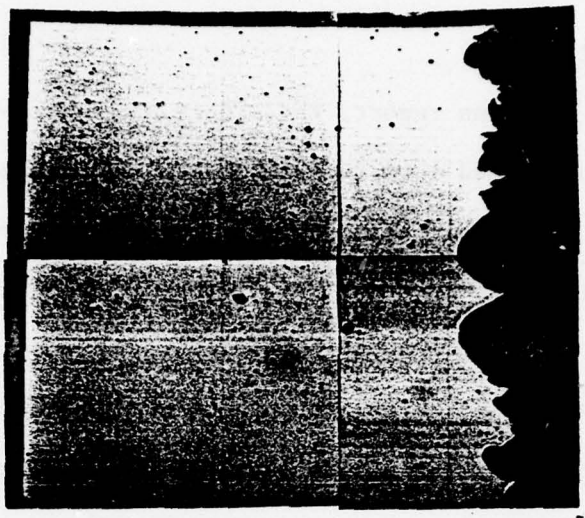


FIG. 6--Acoustic picture of Au on GaAs after annealing at 275°C. 300×.

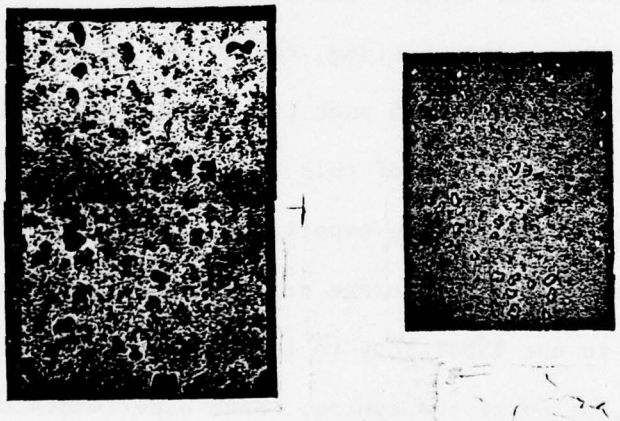


FIG. 7--Pictures of Au on GaAs after annealing at 400°C.
(a) Acoustic 300×; (b) Optical 150×.

III. PROGRESS ON ZnO-on-Si STORAGE CORRELATOR

A. Signal Processing

Since our last progress report, the effort on the ZnO-on-Si storage correlator has been divided into two areas. The first one has been using the existing monolithic correlator to demonstrate the signal processing capability of such a device. Emphasis has been put on the so-called input correlation mode of operation, where signals with time-bandwidth products much larger than the inherent time-bandwidth product of the device can be processed. This particular mode of operation may prove to be very useful in the area of long code recognition. The result of this study was published in last year's November 14th issue of Electronics Letters. A preprint of the paper is attached with this progress report.

Our second effort is to improve the performance of the device toward larger bandwidth, longer time delay, and lower spurious signal levels. The device we are shooting for at the present time is one which has 20 MHz bandwidth, 4-5 μsec time delay, and 50 dB or more dynamic range. Once a device of this kind is made, some more elaborate and practical signal processing experiments will be tried. Included in our plan is to install a storage correlator into one of the acoustic imaging systems in our laboratory to function as an inverse filter to improve the resolution of the system. Such experiments should give us a more realistic evaluation of the potential capability of the storage correlator.

B. ZnO-on-Si Technology

As to the fabrication of this new generation of ZnO-on-Si device, we encountered some technological problems. Samples tested so far failed to produce any usable device. Since the ZnO films have been shown to be of high quality from the RED test, the problem most likely is coming from the Si substrate. Each individual diode in the diode array structure we are presently fabricating is 4 μm and 1 mm long. The separation between diodes is 4 μm. If somehow the samples get contaminated during the processing steps, the surface areas of the regions separating individual diodes will not be maintained at uniform potentials. This may cause inversion layers to form randomly between diodes, thus degrading the performance of the device. To verify this argument, an experiment testing these diode arrays in the airgap configuration is presently underway. At the same time, more diode arrays are being fabricated, taking the precaution that extra cleaning steps are needed to avoid any possible contamination. From our past experience, we feel quite confident that this will be accomplished without any major difficulty.

C. A New Mode of Operation for the Monolithic ZnO-on-Si Storage Correlator

Schematic diagrams of an airgap and monolithic ZnO-on-Si storage correlators are shown in Fig. 8. Two techniques have been used in the past to write a signal into the correlator. The first one is the so-called "flash" technique where a narrow pulse is applied to the center port when the signal fed into transducer A to be stored is propagating underneath the center electrode. The second technique is the RF technique where many cycles of RF voltage which are synchronized with the signal to be stored are applied to the center port. In both cases, all the diodes are momentarily forward

biased so that the signal can be stored in the form of a charge pattern in the diodes.

A second look at Fig.8(b) shows that the same diode array can also be considered as a single gate BBD structure. Suppose now a negative pulse, instead of a positive one, is applied to the gate. Since all the p-type islands in the structure act as sources for holes, the n-type regions in between would be inverted. Like the MOSFETs, the process of inversion layer formation itself can be very fast. If at this moment when inversion occurs, a surface wave is propagating under the gate, then diodes at different positions will be biased at different potentials, depending on the amplitudes of the local electric fields carried by the surface wave. Due to this potential difference, carriers will flow between the p-regions through the conducting layers. Once the charges flow to a p-island they will be trapped there after the gate pulse is switched off. This is how the storage effect is acoomplished.

This idea was tried experimentally. Even though the correlation output is not as good as the best result obtained with the RF technique (5 - 10 dB down) it is reasonable. Figure 9 is the correlation output after 500 μsec a 3 μsec stored RF signal using this BBD technique. The amplitudes of the pulse used is 65 volts.

There is always a chance that the storage effect we are seeing is due to surface states. To check this possibility, the following experiment has been performed. A 2 μsec RF pulse is first stored in the diode array by using the usual RF technique. A negative pulse is then applied to the top electrode before the read-out signal is applied. The argument

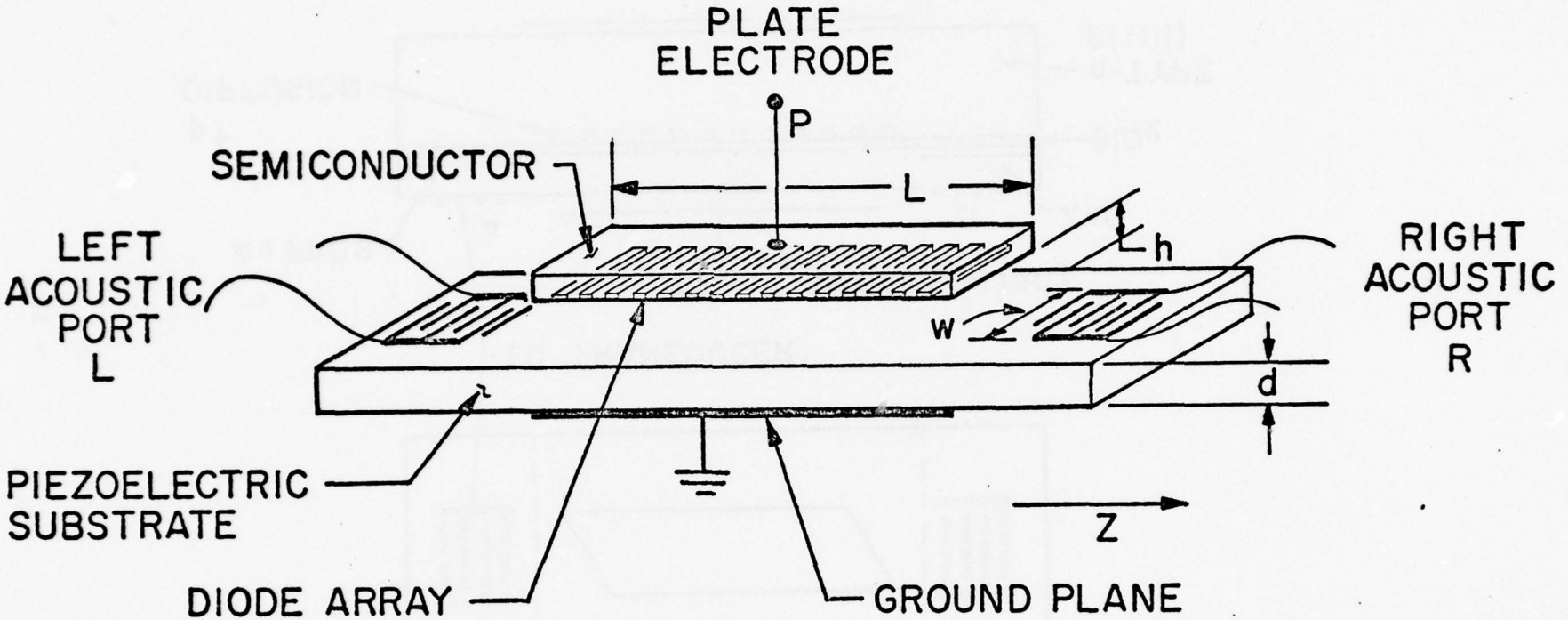


FIG. 8(a)--Typical airgap storage correlator structure.

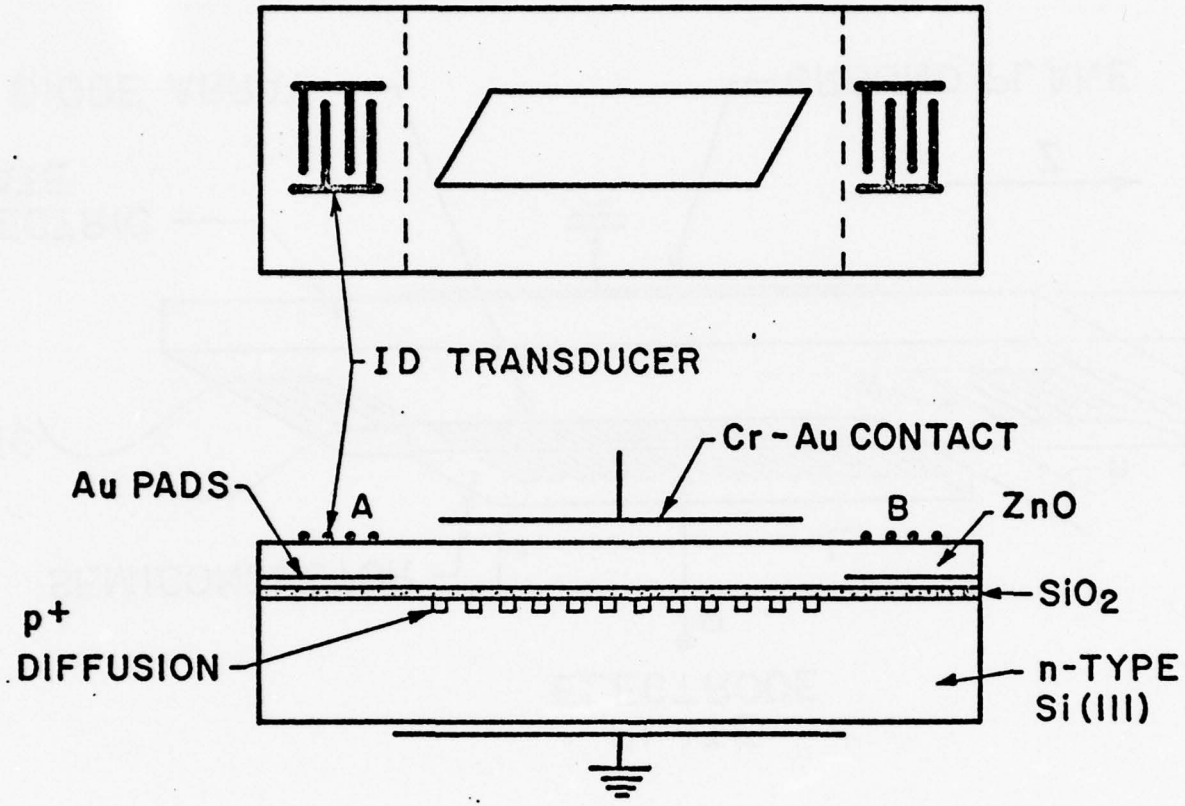


FIG. 8(b)--Typical monolithic storage correlator structure.

is that if indeed the negative pulse is causing charge transfer between diodes, the storage should be erased and no correlation output will be obtained. If the storage effect is because that surface states are being filled or emptied by the negative pulse, then the correlation output should come back after the surface states relax to equilibrium. This would happen because the charges originally stored in the p-regions in general have longer decay time constant than those trapped in the surface states. The experimental result is that a negative pulse does erase the storage. This, to a certain extent, proves that charge transfer between p-regions does occur. Figure 10 shows the correlation outputs with negative pulse being applied before, during, and after the read-out signal. The arrows point out the moments when the pulses are applied.

The detailed principle of the new mode of operation is not totally understood yet at the moment. For example, since the negative pulse is applied to both the p-regions and the n-regions through the same capacitance, it is not clear to us why the potential barrier between the two regions should be lowered to allow the holes to flow to form the inversion layers. In spite of this, the experimental result does point out the possibility of a whole family of new acousto-electric devices, i.e., SAW devices with charge transfer elements.

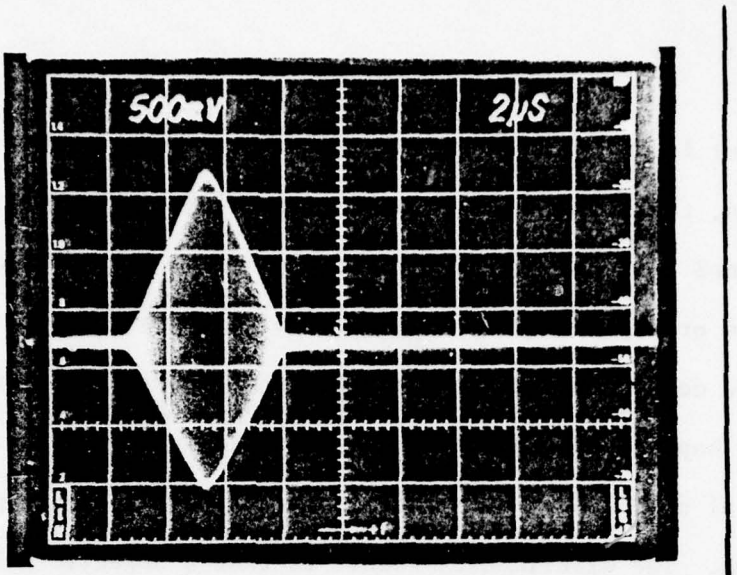


FIG. 9--Correlation output using the BBD technique.

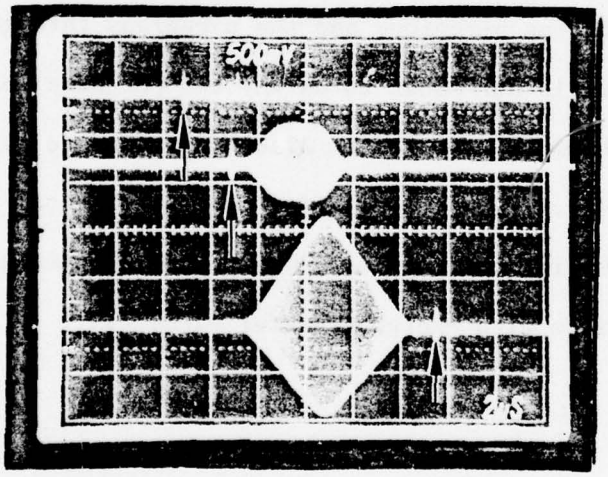


FIG. 10--Erasure of RF storage by a 12 nsec negative pulse.

IV. NEW EXPERIMENTS AND THEORY ON THE CHARGING AND DISCHARGING OF A p-n-DIODE-CAPACITOR SYSTEM

A. Theory of the Process

In Section IIA of the progress report we described the writing of a signal into the SAW storage correlator involves the charging of a capacitor through a series p-n diode. An analytic theory for this charging process was given in our last report in which the theoretical calculation based on this theory was in good agreement in all respects with the experimental results obtained using an airgap storage correlator with a V-groove mesa diode array. However, when a planar diode array instead of a V-groove mesa diode array, was used in the correlation structure, the production on the charging time required was not good. Workers at both Lincoln Laboratory and Thompson CSF in France also encountered the same difficulty in their effort to duplicate the experiment. This led us to have second thoughts on our previous theory concerning the charging mechanism of a p-n diode. As a result, a new theory has been developed and will be presented here.

In order to check the new theory in a more convincing way, the measurement of the charging characteristic of the p-n diode should be isolated from the rather complicated operation of a storage correlator. Large-area diodes were therefore fabricated to which external capacitors and resistors were connected to simulate the storage correlator structure. With this arrangement, the voltages at different points of the circuit can easily be monitored, thus providing a direct measurement of the charging characteristics of the p-n diode. It also has the flexibility

that the external capacitor and resistor can be changed readily so that their effects can be studied.

The following treatment is broken into three sections. In the first section the new charging theory for the p-n diode is discussed. The second deals with the discharging periods of the diode. In the third section, the experimental procedures will be examined and comparisons between the theory and the experiment will be made.

(1) The Charging of a p-n Diode by a Narrow Pulse

Typical airgap and monolithic storage correlator structures to which the present theory will be eventually applied are schematically shown in Fig. 8. The equivalent circuit looking into the center port is essentially a p-n diode in series with a capacitor and a resistor, as shown in Fig. 11. The capacitor represents the capacitance of the $LiNbO_3$ delay line in the airgap case, and that of the ZnO film in the monolithic case. The resistor is due to the output impedance of the driving pulser, the lead resistance, and the bulk resistance of the Si substrate. Although the theory presented here is general enough to cover driving sources (V_s) of arbitrary waveform and duration, we will focus on the use of a single narrow pulse because this is more pertinent to our actual experiment set-up with the storage correlator.

Originally before application of an external potential the diode is in thermally equilibrium with a built-in barrier potential of V_B volts. After the source is turned on, the depletion capacitance of the diode is charged up and diode becomes forward biased. Under this forward bias condition, minority carriers (holes) are passed from the p-region through

the depletion region into the n-region. This process is transit-time limited and requires only a few tens of picoseconds. Once the minority carriers are in the n-region, they start to diffuse into the bulk and at the same time recombine with the majority carriers at a certain rate, as determined by their lifetime. The total number of minority carrier swept into the n-type substrate is related to the forward bias and will rise as the diode is increasingly forward biased by the rising pulse. The extent of the forward bias, as well as the total number of minority carrier in the n-region, are limited by the external circuit.

After the pulse has reached its peak and starts to decay, the voltage across the diode will also be going down. This, in turn, forces the minority carrier density at the edge of the depletion layer to drop. Once this happens, the minority carriers already in the n-region can diffuse both ways, either into the bulk or toward the depletion layer. The holes which reach the depletion layer will be swept right back to the p-region, where they originally came from. Eventually, in a matter of a few microseconds, all the minority carriers except those which have recombined with the majority carriers will be brought back to the p-side of the junction. The minority carriers which have recombined represent the net amount of charge lost by the p-region during this charging process. They can only be resupplied slowly by the small reverse saturation current of the diode. This, depending on the magnitude of the reverse current, may last from tens of milliseconds to a few seconds. It therefore represents a storage effect. *It is the concept that only the recombined*

minority charges can contribute to the storage that marks the main difference between the present theory and the previous theory.

Following the discussions above, the diode can properly be modeled as shown in Figs. 11 and 12. C_{dep} which depends on the junction voltage, is the depletion capacitance of the diode $Q_p(t)$ is the total amount of minority carrier charge stored in the neutral region and τ_p is the minority carrier lifetime. Thus, the total current entering the neutral region is

$$I = \frac{\partial Q_p}{\partial t} + \frac{Q_p}{\tau_p} \quad . \tag{1}$$

$Q_p(t)/\tau_p$ is the instantaneous recombination current through the diode, and $\partial Q_p(t)/\partial t$ is the charging current.

The total charge $Q_p(t)$ due to the presence of minority carriers in the n-region, is related to the junction voltage $V(t)$ through the diffusion equation

$$D_p \frac{\partial^2 p(x,t)}{\partial x^2} - \frac{p(x,t)}{\tau_p} = \frac{\partial p(x,t)}{\partial t} \tag{2}$$

where $p(x,t)$ is the excess minority carrier density and D_p is the diffusion constant for holes.

The proper boundary conditions for Eq. (1) are

1. $p(0,t) = P_{n0}(e^{\beta V(t)} - 1)$,
2. $p(x,0) = 0$,
3. $p(\infty,t) = 0$

where $x = 0$ is chosen to be at the edge of the depletion layer as shown

in Fig. 13. p_{n0} is the hole concentration in the bulk n-region and $\beta = q/kT$. Using Laplace transform technique, the solution to Eq. (1) with the proper boundary conditions is found to be

$$p(x,t) = \frac{x}{2\sqrt{D_p \pi}} \int_o^t P_{n0}(e^{\beta V(\tau)} - 1) \frac{e^{-(t-\tau)/\tau_p}}{(t-\tau)^{3/2}} e^{\frac{-x^2}{4D_p(t-\tau)}} d\tau \ . \quad (3)$$

As can be seen, the minority carrier distribution at any time t not only depends on the bias across the junction at that instant but also depends on the past history of the diode.

The total charge due to the minority carriers, $Q_p(t)$, can then be found:

$$Q_p(t) = \frac{1}{\sqrt{\pi}} \int_o^t I_s \underbrace{\left[e^{\beta V(\tau)} - 1\right]}_{I} \underbrace{\frac{e^{-(t-\tau)/\tau_p}}{\left(\frac{t-\tau}{\tau_p}\right)^{1/2}}}_{II} d\tau \quad (4)$$

where $I_s = q\sqrt{D_p/\tau_p}$. This equation is of the convolution form and it can clearly be seen that I is the driving term and II is simply a weighting factor. It states that the contribution to the total minority carrier charge at time t from a previous bias on the diode at time τ is scaled down by a weighting factor depending on the ratioo of the elapsed $t - \tau$ to the minority lifetime τ_p .

The total minority charge recombined at the end of the charging process

$$Q_R = \int^{\infty} \frac{Q_p(t)}{\tau_p} dt = \iint^{\infty} \frac{I_s}{\sqrt{\pi \tau_p}} \left(e^{\beta V(\tau)} - 1\right) \frac{e^{-(t-\tau)/\tau_p}}{\left(\frac{t-\tau}{\tau_p}\right)^{1/2}} d\tau \quad (5)$$

This is the integral which is of the most interest to us and it has to be calculated eventually.

Equation (4) can now be used to set up the loop equation for the equivalent circuit in Fig. 14. The resultant equation obtained is given below:

$$V_S(t) = V(t) + B\left(1 - \sqrt{1-V(t)V_B}\right) + \frac{D}{\sqrt{1-V(t)/V_B}} \frac{dV(t)}{dt}$$

$$+ E\int_o^t \left(e^{\beta V(\tau)}-1\right) \frac{e^{-(t-\tau)/\tau_p}}{\left[(t-\tau)/\tau_p\right]^{1/2}} d\tau$$

$$+ F\int_o^t V(\tau)e^{\beta V(\tau)} \frac{e^{-(t-\tau)/\tau_p}}{\left[(t-\tau)/\tau_p\right]^{1/2}}$$

$$+ G\int_o^t\int_o^t \left(e^{\beta V(u)}-1\right) \frac{e^{-(\tau-u)/\tau_p}}{\left[(\tau-u)/\tau_p\right]^{1/2}} du\, d\tau \qquad (6)$$

where

$$B = \frac{A\sqrt{2q N_d V_B}}{C}$$

$$D = AR\sqrt{\frac{qN_d}{2V_B}}$$

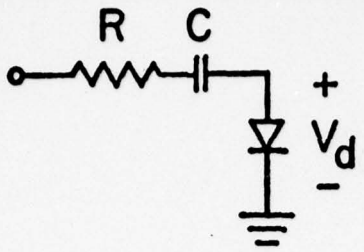


FIG. 11--Equivalent circuit looking into the top electrode of the storage correlator.

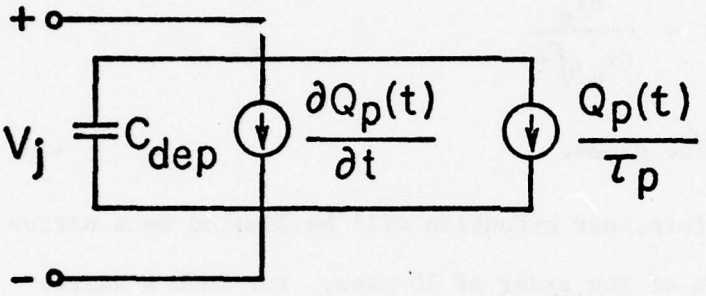


FIG. 12--Transient analysis model for a p-n diode.

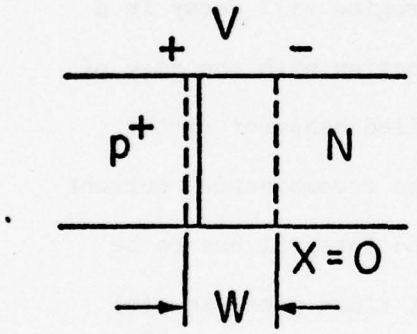


FIG. 13--One dimensional p-n diode geometry for solving diffusion equation.

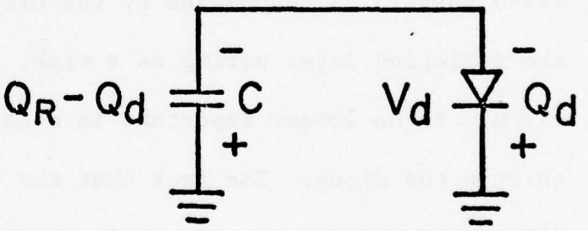


FIG. 14--Equivalent circuit of a p-n diode under reverse bias.

$$E = \frac{AI_s}{\sqrt{\pi}} (R/\tau_p + 1/C)$$

$$F = \frac{A\beta RI_s}{\sqrt{\pi}}$$

$$G = \frac{AI_s}{C\tau_p \sqrt{\pi}}$$

and A is the area of the diode.

As we mentioned before, our attention will be limited to a narrow driving pulse with width of the order of 10 nsec. For such a narrow pulse, the voltage across the diode in general will stay positive only for approximately the same period of time. Once the diode is reverse biased, the minority carriers trapped in the n-region will decay in a fixed pattern as determined by the diffusion equation with the edge of the depletion layer acting as a sink. The detailed behavior of the circuit is no longer important in determining the recombination current through the diode. The fact that the convolution integral has to be calculated only for a relatively short period of times makes Eq. (6) easily accommodated in a computer program.

The computer program basically solves Eq. (6) iteratively to find the junction voltage and the total stored minority charge as a function of time. This calculation will terminate once the junction voltage becomes negative. From this point on, only Eq. (4) is needed to determine the behavior of the stored minority charge. Though it is not a totally

trivial form Eq. (4), Q_p will decay rather sharply right after the junction voltage passes its peak value. This decay will slow down gradually and eventually for large t, $Q_p(t)$ can be expressed in a much simpler form.

$$Q_p(t) \approx \frac{1}{\sqrt{\pi}} \frac{e^{-t/\tau_p}}{(t/\tau_p)^{1/2}} \int_0^t I_s \, e^{\beta V(\tau)} - 1) d\tau \tag{7}$$

$$= Q_o \frac{e^{-t/\tau_p}}{(t/\tau_p)^{1/2}}$$

where $Q_o = \frac{1}{\sqrt{\pi}} \int_o^{T_0} I_s \left(e^{\beta V(\tau)} - 1 \right) d\tau$ and T_0 is the instant when the junction voltage becomes negative. Thus Q_0 is the charge initially stored in the natural region.

For the short pulse we are using, Eq. (7) will be a valid approximation for $t \geq 60$ nsec. To find the total charge recombined at the end of the charging process, we simply calculated the following integral

$$Q_R = \int_0^{\infty} \frac{Q_p(t)}{\tau_p} = \int_0^{60 \text{ nsec}} \frac{Q_p(t)}{\tau_p} dt + \int_{60 \text{ nsec}}^{\infty} \frac{Q_p(t)}{\tau_p} dt \tag{8}$$

using Eqs. (4) and (7).

The results of this calculation will be shown in Section 2.

(2) Discharging of the Stored Charge

As we explained in Section 1, an amount of charge Q_R is stored in the diode-capacitor system after the charging process. This stored

charge will be discharged slowly through the reverse leakage current of the diode. Since the reverse leakage current of a p-n diode is usually very small, the resistor in the circuit of Fig. 11 can always be neglected and the equivalent circuit becomes simply as that shown in Fig. 14.

The total charge Q_R stored in the system has to redistribute itself in such a way that the potential drop across the capacitor is equal to that across the diode, i.e.,

$$\frac{Q_R - Q_D}{C} = V_d \tag{9}$$

where Q_d is the extra depletion layer charge needed to reverse bias the diode voltage of V_d .

For a p-n junction in thermal equilibrium,

$$V_B = \frac{qN_d x_0^2}{2\varepsilon} = \frac{(qN_d x_0)^2}{2q\varepsilon N_d} = \frac{Q_0^2}{2aN_d\varepsilon} \tag{10}$$

where x_0 and Q_0 are the depletion layer width and the depletion layer charge, respectively, under zero bias condition.

With a reverse bias of V_d volts, an extra amount of charge Q_d is residing in the depletion layer, and Eq. (10) becomes

$$V_B + V_d = \frac{(qN_d x_n)^2}{2\varepsilon qN_d} = \frac{(Q_0 + Q_d/A)^2}{2\varepsilon qN_d} \tag{11}$$

where A is the area of the diode. Therefore,

$$V_d = \frac{(Q_0 + Q_d/A)^2}{2\epsilon q N_d} - V_B = \frac{Q_d/A\ Q_d/A + 2\ \sqrt{2qN_d\ V_B}}{2q\epsilon N_d} \qquad (12)$$

Substituting Eq. (12) into Eq. (9), we find that

$$Q_d = \frac{-(\beta+1/\alpha) + \sqrt{(\beta+1\alpha)^2 + 4Q_R/\alpha}}{2} \qquad (13)$$

where $\alpha = \frac{C}{2q\ N_d A^2}$, $\beta = 2A\sqrt{2q\epsilon N_d V_B}$.

The reverse bias on the diode can therefore be found through Eq. (12) by writing

$$V_d = \frac{\alpha Q_d (Q_d + \beta)}{C} \quad . \qquad (14)$$

The stored charge Q_R will leak away through the reverse saturation current of the diode and, as a result, the reverse bias on the diode will decay slowly toward zero. The expression governing this decay will be derived below.

The reverse current of a diode is in general bias dependent. For most cases, the thermally generated carrier in the depletion layer constitute the dominant source for this reverse current. We assume that this applies to our diodes, too.

$$I_{gen} = \frac{1}{2}\ \frac{qn_i}{\tau_0}\ WA = \frac{1}{2}\ \frac{qn_i}{\tau_0}\ A\sqrt{\frac{2\epsilon}{qN_d}\ (V_d + V_B)} \qquad (15)$$

where n_i is the intrinsic carrier concentration, τ_0 is the carrier lifetime, and W is the depletion layer width.

The rate of change of the voltage across the diode can therefore be written in the following simple form

$$\frac{d(V_d/V_B)}{dt} = - \frac{n_i}{N_d} \frac{1}{\tau_0} \frac{1 + V_d/V_B}{1 + M(1 + V_d/V_B)^{1/2}} \tag{16}$$

where $M = \frac{C}{A}\sqrt{\frac{2V_B}{qN_d}} = \frac{C}{C_0}$ is the ratio of the external capacitance to junction capacitance at zero bias.

The solution to Eq. (16) is

$$\ln \frac{1 + V_d(t)/V_B}{1 + V_d(0)/V_B} + 2M\left(\sqrt{1 + V_d(t)/V_B} - \sqrt{1 + V_d(0)/V_B}\right) = - \frac{t}{T} \tag{17}$$

where $T = \frac{N_d \tau_0}{n_i}$

According to Eq. (17), the decay characteristic of a charged-up diode-capacitor system not only depends on the leakage current of the diode, it also depends on the initial value of the reverse bias and the ratio of the external capacitor to the junction capacitance.

(3) Experimental Results

Figure 15 is a schematic diagram of the experimental set-up. The high impedance probe at point A measures the amplitude of the pulse actually driving the circuit. The probe across the diode measures the

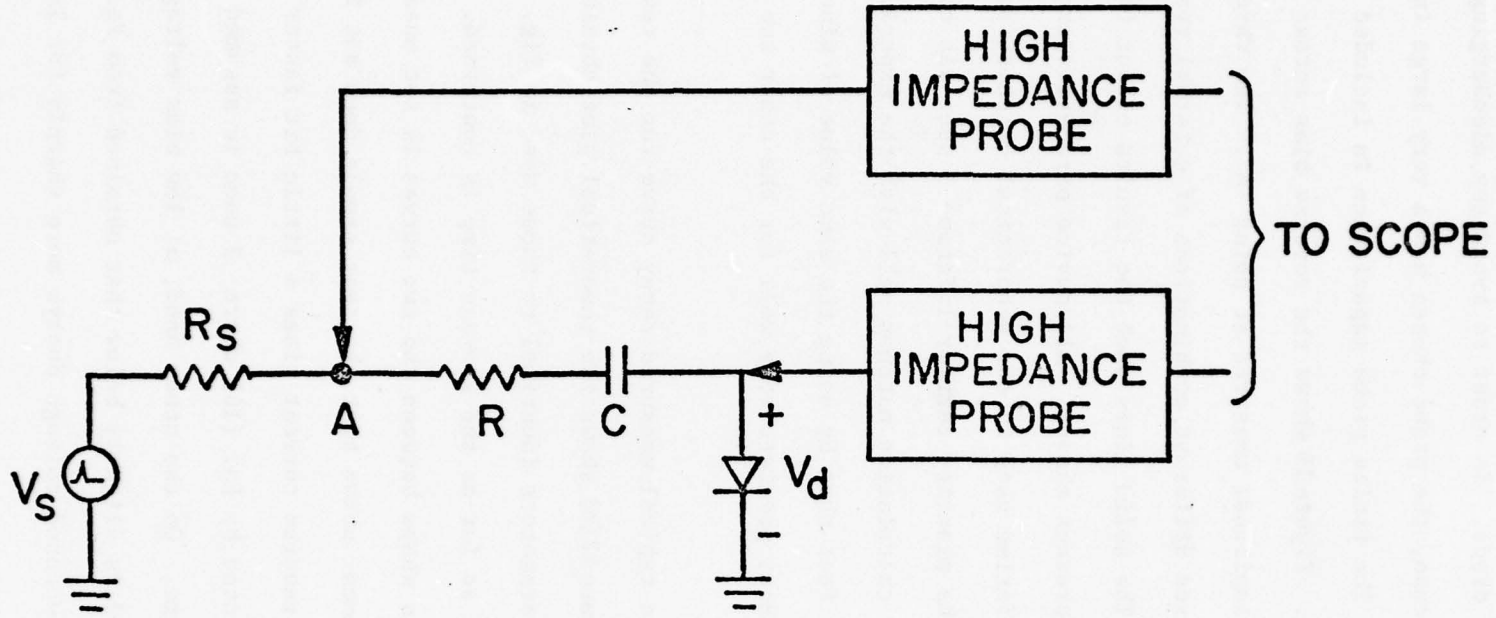


FIG. 15--Experimental set-up for studying the charging and discharging of a p-n diode.

reverse bias across the diode. In order to avoid any discharging of the capacitor through the scope, the probe chosen has a very large input impedance ($>10^{12}\Omega$) . The finite probe capacitance is included in the theoretical calculation. Figure 16 shows the reverse bias across the diode versus the pulse amplitude measured at point A . The three curves correspond to three different combinations of external resistor and capacitor values. The solid lines show the results of our theoretical calculations using the present theory. All device parameters except the minority carrier lifetime used in our theoretical calculations are measured quantities. The minority carrier lifetime 3 μsec was chosen so that the theoretical calculation matches well with the experimental result in case II. The fact that by using the same value of minority carrier lifetime the theory predicts very well for the other two cases is very encouraging.

Figure 17(a) shows a typical measured decay curve for the reverse bias on the diode. Figure 17(b) shows the theoretical plot obtained using Eq. (17) with devices parameters identical to those used in Fig. 16. The agreement is quite good so far as the storage time is concerned. The noticeable difference in shape between the two curves is not unexpected. The reverse I-V measurement shows that the test sample does not follow Eq. (15) exactly. The reverse current rises a little bit faster with reverse bias than predicted by Eq. (16) where 3 μsec is assumed for the minority carrier lifetime. On the other hand, at low bias voltage the leakage current measured is slightly below that obtained from Eq. (16). This explains why the measured voltage decays more sharply for large

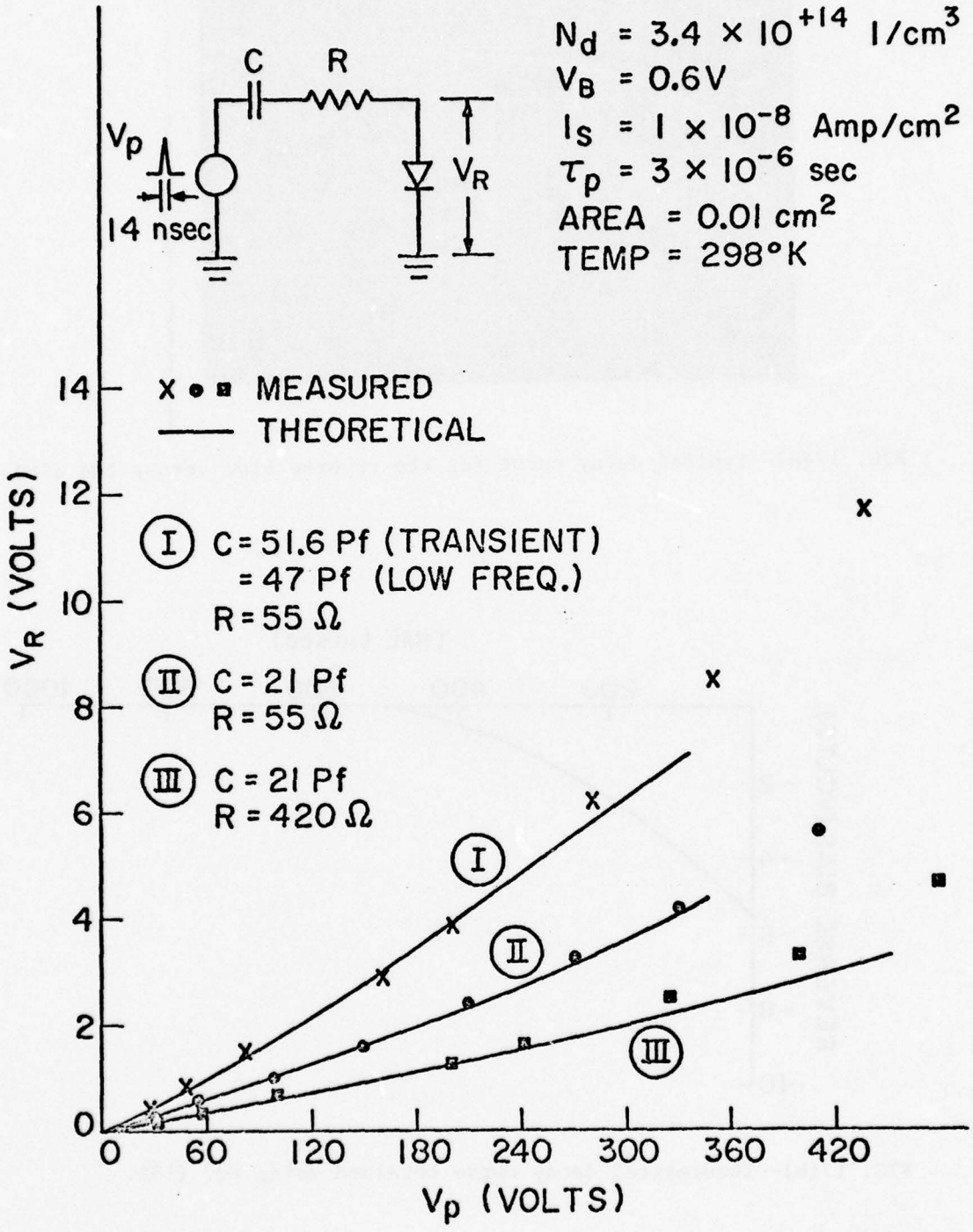


FIG. 16--The reverse bias across the p-n diode after charging vs the amplitude of the narrow charging pulse.

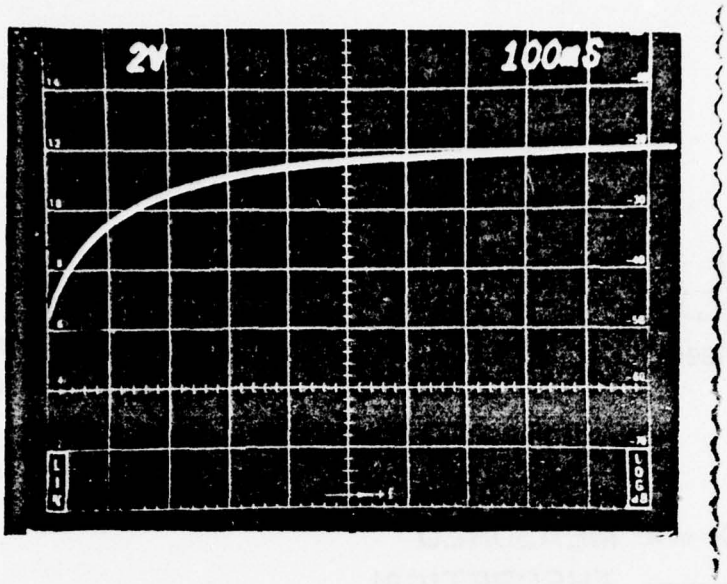


FIG. 17(a)--Typical decay curve for the reverse bias across the diode.

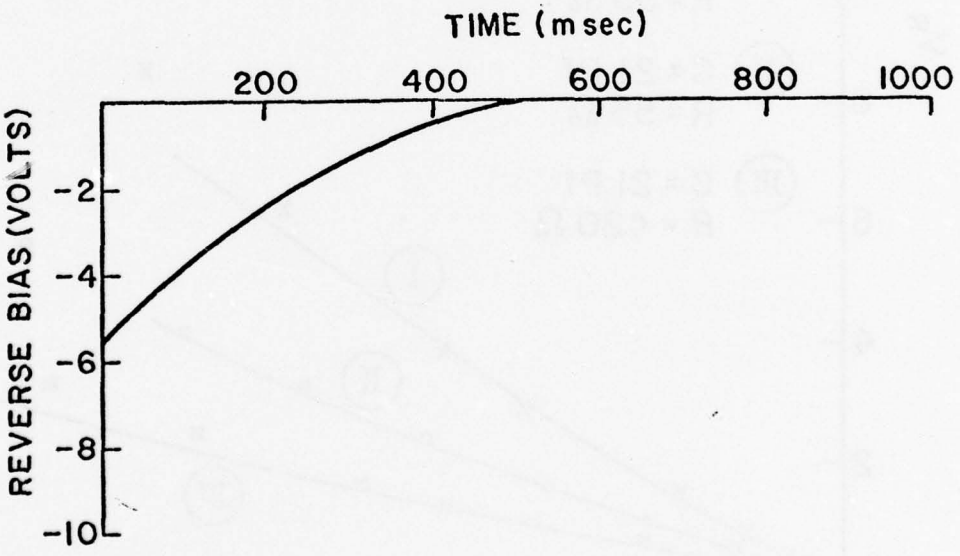


FIG. 17(b)--Theoretical decay curve obtained using Eq. (18).

reverse bias and more slowly for low reverse bias. The agreement in storage time between the theory and the experiment also suggests that the choice of 3 μsec as the minority carrier lifetime is a reasonably good one.

We see that the theory predicts the behavior of a p-n diode reasonably well under conditions normally ised in a p-n diode correlation. It would appear that our V groove p-n diodes had far shorter recombination times than had originally been thought. This would explain how we were able to charge them almost fully with a relatively short pulse a few nanoseconds long. It would also explain why in experiments with longer sotrage time diodes, longer charging times were required.

We have reexamined the storage output from an airgap correlator containing a silicon diode array that was 1 3/4 years old; this array had not been thermally oxidized and only a native oxide was used in much the same manner as in the base silicon convolvers made here and at Lincoln Labs. It was found that the storage output had decreased by 20 dB and the 3 dB storage time had decreased from 8 ms to 450 us, although the efficiency as a convolver had not changed.

The diodes in this case were p+/n V grooved diodes with unoxidized surfaces. It was found that by applying a 500 v forward bias across the diodes, the efficiency could be increased to its former value and the storage time could be increased by a factor of 30 to 1 ms. This is twice as long as was measured a year and one half ago.

We believe the deteriorating effect was due to the change in surface potential as a result of contamination or increased oxidation on the V-groove

surfaces. The forward bias then removed the inversion layer at the surface. The remedy should be simple, to thermally oxidize the silicon after construction of the array.

It should be noted that calculations of the type given here would need relatively short recombination times of the order of 3 μsec to give a storage time as short as 8 msec. In this case the storage could be carried out with a short pulse, as we had found earlier.

APPENDIX A

AN ANALYTIC THEORY OF THE DIODE STORAGE CORRELATOR

This Appendix is Chapter IV of a long report which is being written and is included to give a detailed description of the theory of the storage correlator which has been developed.

LIST OF VARIABLES

( ) Equation number where variable is defined or first used

a: Spacial dependence of fundamental acoustic mode (49)

C: Reduced model coupling capacitance, $= C_a + C_p$ (4)

C_a Acoustic coupling capacitance (1)

C_D: Diode capacitance (9)

C_{DO}: Diode capacitance for $V_D = 0$ (8)

C_{Dp}: Peak diode capacitance for pulse writing (14)

C_{ov}: Overlay capacity (60)

C_p: Plate circuit coupling capacitor (4)

C_T: Total capacity, $= C + C_D$ (12)

C_{Tp}: Peak total capacity, $= C + C_{Dp}$ (14)

d: Piezoelectric substrate thickness

D_p: Minority carrier diffusion constant (A-1)

E_g: Semiconductor bandgap energy

f: filling factor (B-1)

h: Airgap thickness (1)

I_a: Current in acoustic circuit (3)

I_D: Total diode current (3)

I_n: Readout current through n^{th} diode element (43)

I_p: Current in plate circuit (3)

I_s: Diode reverse saturation current (7)

k: Boltzmann's constant (7)

ℓ: Diode array periodicity, (56)

L: Length of interaction region (44)

$\mathcal{M}_c$: Efficiency of acoustoelectric convolver (57)

$\mathcal{M}_{sc}$: Efficiency of storage correlator (56)

$M(\beta h)$: Space charge coupling factor (B-3)

n_i: Intrinsic carrier density

N: Number of diode elements per unit length (44)

N_D: Semiconductor doping density (8)

$p_n(x,t)$: Minority carrier density in neutral region (A-1)

P_{n0}: Equilibrium minority carrier density (41)

P_{ar}: Acoustic reading signal power

P_{aw}: Acoustic writing signal power

P_0: Output power (reading) (45)

q: Electron charge (7)

Q_R: Readout charge

Q_{RD}: Component of Q_R stored in the diode capacitor, C_D (61)

Q_D: Total charge in the diode capacitor, C_D (8)

Q_0: Component of stored charge without spacial phase βz (40)

Q_p: Excess minority carrier charge in neutral region (A-4)

Q_s: Total stored charge, $Q_s = Q_0 + Q_a$ (11)

R_a: Series resistance in acoustic circuit

R_L: Output load resistance (44)

R_p: Series resistance in plate circuit

t: Time (13)

t_p: Time of peak of writing pulse (13)

T: Temperature (7)

T_p: Minority carrier recombination time constant (A-1)

v_a: Acoustic propagation velocity

V_{aw}: Potential due to acoustic writing signal (5)

V_{a0} Modulation of V_{aw} (13)

V_{awl},V_{aw2}: Acoustic writing potential (acoustic-acoustic mode)

V_B: Built-in diode junction voltage (8)

V_D: Diode voltage (8)

V_{Dp}: Peak diode voltage during pulse writing (19)

V_{Dr}: Diode voltage component exciting readout (acoustic-to-plate mode) (42)

$V_{Dr}^{\pm}$: Diode voltage component exciting readout (plate-to-acoustic mode) (55)

V_{Dr0}: Coefficient of Floquet expansion of $V_{Dr}^{\pm}$ (56)

V_L: Voltage developed across output load resistor, R_L (43)

V_{on}: Turn-on voltage (21)

V_{po}: Peak amplitude of plate writing signal (18)

V_{pw}: Potential due to plate writing signal (5)

V_s: Reduced model source voltage (5)

w: acoustic beam width (6)

z: Position along diode array (49)

z_n: Position of n^{th} diode array element (48)

Z_a: Acoustic impedance (6)

β: Acoustic propagation constant

δ: Diode array element width (1)

ε_0: Dielectric constant of air (1)

ε_p: Dielectric constant of piezoelectric (2)

ε_s: Dielectric constant of semiconductor (8)

γ: Perturbation in β due to presence of semiconductor (52)

ω: Radial frequency

ϕ: Total acoustic potential seen in space above piezoelectric,
$= \phi_a + \phi_s$ (51)

ϕ_1: Fundamental term in harmonic expansion of acoustic potential (49)

ϕ_a: Potential due to fundamental propagating acoustic mode (51)

ϕ_s: Potential due to all other acoustic modes (50)

ϕ_{ar}: Readout surface wave potential (39)

ϕ_{pr}: Plate reading potential (45)

ρ_s: Semiconductor surface charge density due to ϕ_s (50)

$|\Delta v/v_a|$ Measure of coupling to piezoelectric substrate (6)

The acoustoelectric surface wave storage correlator is a device capable of storing and correlating broad bandwidth signals in real time. Considerable development has occurred since the first demonstration of principle, and a number of device structures and modes of operation have evolved. Here, we derive an analytic theory broad enough in scope to elucidate the physics and accurately predict the performance of most of the reported structures and modes of operation.

The device considered consists of a silicon diode array situated a few hundred nanometers above an acoustic acoustic surface wave delay line, as shown in Fig. 1. It has three ports: two connected to acoustic surface wave transducers, (L,R) , and a third, called the plate (P) , connected to the back of the diode array. The interaction of inputs from any two of the ports writes a signal into the diode array in the form of a spacially varying charge pattern. A later input, called the readout signal, causes a readout to appear at one of the three ports in the form of a correlation or convolution of the readout signal and the stored charge pattern.

The process of writing a charge pattern into the diode array may be understood with the aid of Fig. 2(a). The equivalent circuit for a single element of the diode array consists of a diode connected to a voltage source V through a coupling capacitor C_p . Let us first consider the case where the source voltage V is a single large short duration voltage spike of peak amplitude V_{pk} . The diode will rapidly turn on and act essentially like a closed switch, so that a charge $Q_s = C_p V_{pk}$ is deposited in the coupling capacitor C_p . When the pulse returns to zero, the capacitor C_p appears

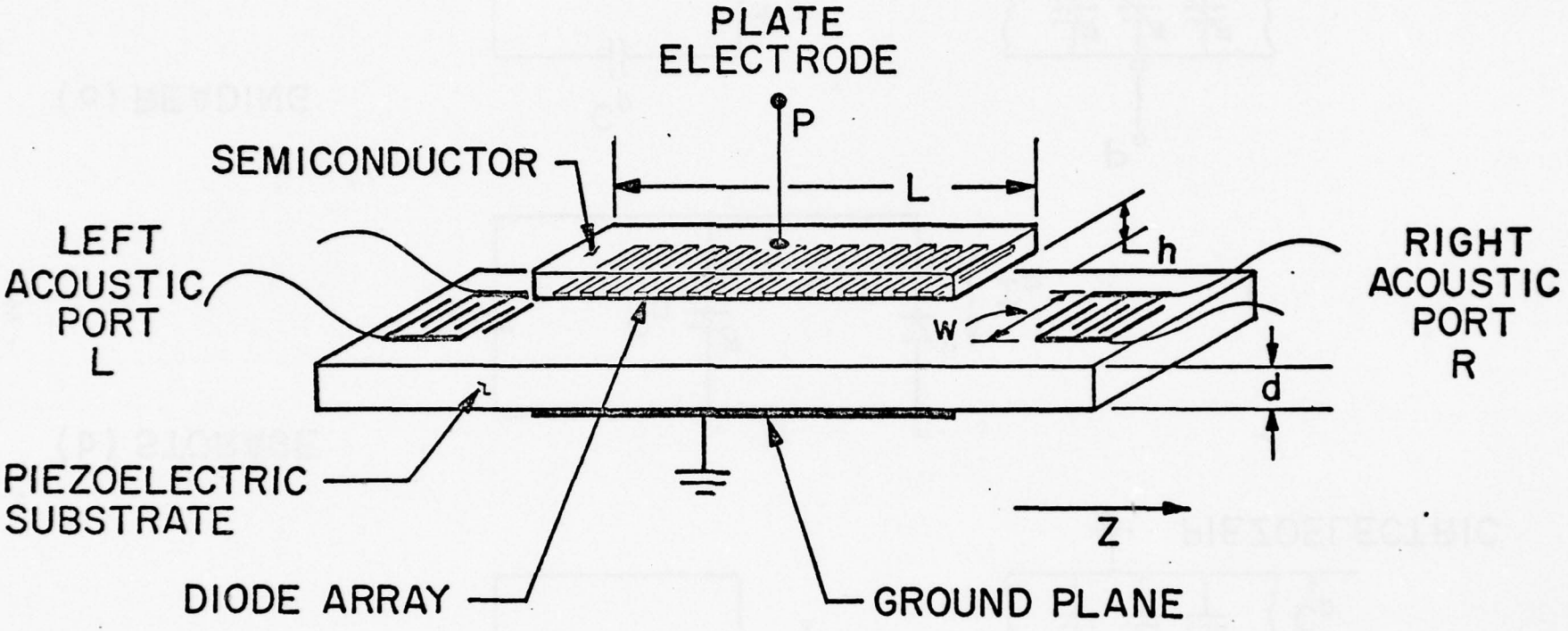
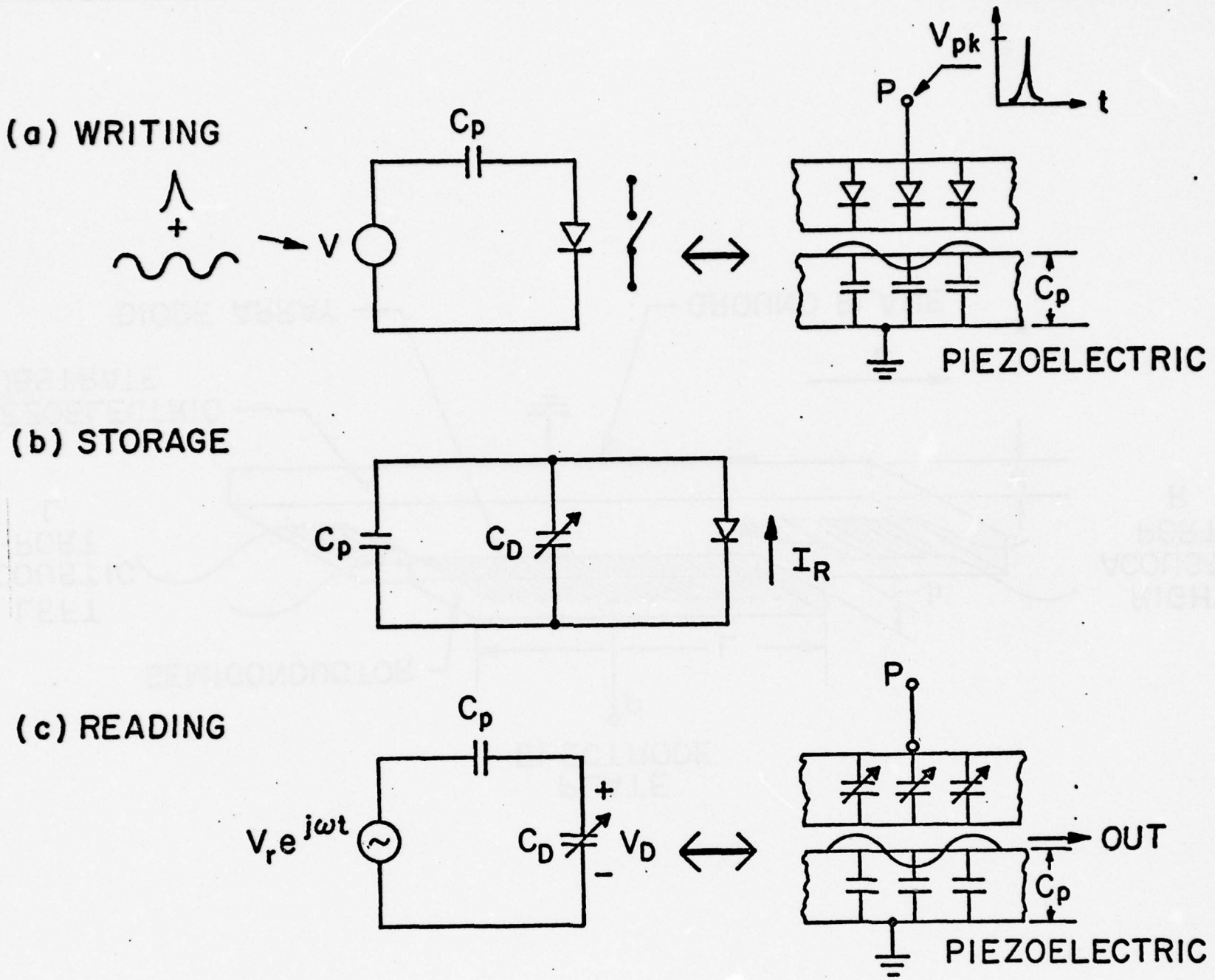


PLATE
ELECTRODE
P
SEMICONDUCTOR
L
h
LEFT
ACOUSTIC
PORT
L
RIGHT
ACOUSTIC
PORT
R
W
d
PIEZOELECTRIC
SUBSTRATE
Z
DIODE ARRAY
GROUND PLANE


(a) WRITING
C_p
V
V_{pk}
P
t
C_p
PIEZOELECTRIC
(b) STORAGE
C_p
C_D
I_R
(c) READING
C_p
$V_r e^{j\omega t}$
C_D
V_D
+
−
P
OUT
C_p
PIEZOELECTRIC

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across the diode, reverse biasing it. The stored charge Q_s now leaks out of the capacitor C_p very slowly, with the diode reverse leakage current, Fig. 2(b).

If an acoustic surface wave travels on the piezoelectric substrate under the diode, its associated electric fields will bias the diode. In this case, the source voltage V is the sum of two components, a dominant one due to the plate pulse, and a smaller one due to the surface wave. When the plate pulse turns on the diode, a small component of the charge deposited and stored in the coupling capacitor C_p is due to the surface wave amplitude at the position of the diode. In this manner, information contained in the surface wave may be stored as a charge pattern in the diode array.

Readout may be obtained by applying an rf reading signal $V_r e^{j\omega t}$ to the plate, as in Fig. 2(c). This reading signal appears across the capacitive voltage divide composed of the diode varactor C_D and the capacitance due to the piezoelectric substrate thickness C_p. The diode capacitance C_D is a function of the stored charge Q_s, so that a component of the diode voltage V_D is due to the product of the stored charge and the reading signal. This component excites a surface wave that is seen at the surface wave transducers as either the convolution or correlation of the readout signal and the stored charge pattern.

In reality, the device operation is far more complex. There are a number of alternate modes of writing and reading, and a number of device structures. We will shortly consider the unique features of each case in detail.

The first version of the storage correlator, reported in 1974 by Cafarella and Bers [1], and also by Hayakawa and Kino [2], employed silicon surface state storage. In 1975, Ingebrigtsen [3] demonstrated the first device with Schottky

diode storage. Soon afterward, Maerfeld and Tournois [4], and also Borden and Kino [5], reported results with devices employing storage in arrays of p-n junction diodes. In general, diode storage has proven far superior to surface state storage with respect to reproducibility, storage time, efficiency and uniformity. This motivates restricting the scope of this paper to the diode correlator; indeed, most current devices employ arrays of either Schottky or p-n junction diodes as the storage medium.

Past theoretical treatments have considered the storage of signals in surface states [6], or of low level input signals in diodes [7],[8],[9]. Here, we address the need for a general theory, wherein the performance of the device is predicted when any reported method of writing a signal into the diode array is coupled with any reported readout technique. Furthermore, our results are always provided in analytic form to enable their ready use in the understanding or design of a storage correlator. The assumptions thus required in most cases minimally affect the final accuracy; we will make note when this is not the case.

This work is broken into five parts. The first one catalogues the various modes of operation and diode array structures herein considered. The second section deals with the writing of a signal into the diode array. We adopt appropriate circuit models and, in each case, calculate the net stored charge residing in the diode array at the end of the writing process. In the third section, we establish circuit models appropriate for readout and calculate the device output in terms of the stored charge found in Section 2. A fourth section is devoted to a comparison with experimental results. In the final section we consider the relative performance of the various device structures and modes of operation, and compare the storage correlator's efficiency to that of other existing acoustoelectric signal processing devices.

1. Modes of Operation and Diode Array Structures

The storage correlator's operation involves two distinct processes. The first of these, called "writing", is the operation of storing a signal in the diode array as a spacially varying charge pattern. The second, called "reading", is the correlation or convolution of the stored charge pattern with a readout signal. The various modes of writing and reading considered here are summarized in Fig. 3 and Table I.

In acoustic-plate writing, the electric fields associated with a traveling surface acoustic wave interact with an externally applied plate signal to charge the diodes. We consider separately the two alternate cases where the plate signal is either a large amplitude, short duration voltage pulse or a low level rf signal. In acoustic-acoustic writing, a second surface wave input signal replaces the plate signal.

Two reading modes are considered. In acoustic-to-plate reading, the readout signal is applied to one of the acoustic ports and the output appears as an rf signal at the plate terminal. In plate-to-acoustic reading, the readout signal is applied to the plate and the output appears at one of the acoustic ports. As indicated in Fig. 3 and Table I, the time inverse readout functions of correlation and convolution are obtained by appropriate choice of the acoustic port.

Before quantitatively describing the theory of operation, it is helpful to gain some physical insight into the processes involved. Reference is made to the simplified circuit models of Fig. 4. The circuit model of Fig. 4(a), which functions essentially like a sample and hold circuit, is appropriate for acoustic-plate writing when the external signal is a single high amplitude pulse. The sampling capacitor, C , is due to both the airgap

TABLE I

Writing

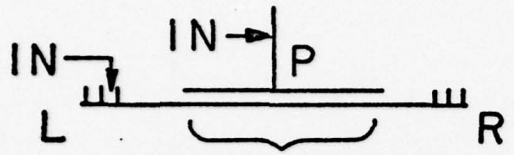
Mode	Input Ports	Spacial Phase of Stored Pattern
Acoustic-Plate	L,P (either single pulse or rf)	βz
Acoustic-Acoustic	L,R	$2\beta z$

Reading

Mode	Input Port	Readout Port	Readout
Acoustic-to-plate	L	P	Correlation
	R	P	Convolution
Plate-to-Acoustic	P	L	Correlation
	P	R	Convolution

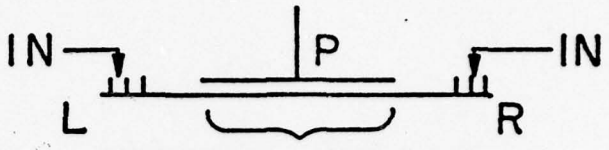
(a) WRITING

ACOUSTIC - PLATE



STORED CHARGE PATTERN (β)

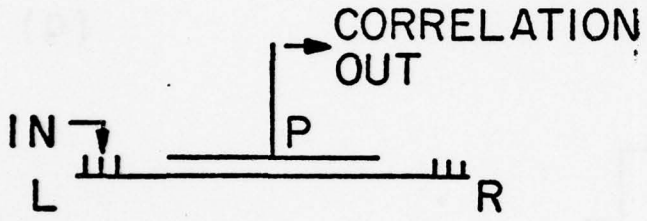
ACOUSTIC - ACOUSTIC



STORED CHARGE PATTERN (2β)

(b) READING

ACOUSTIC - TO - PLATE



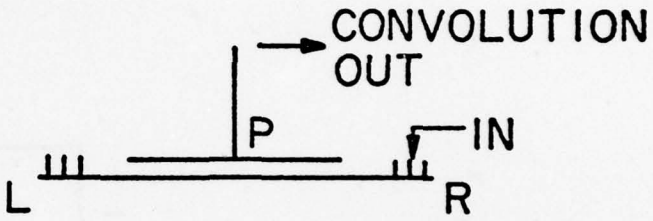
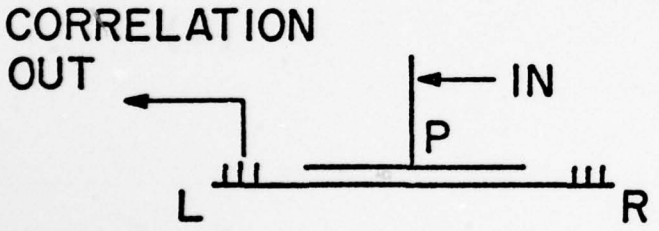
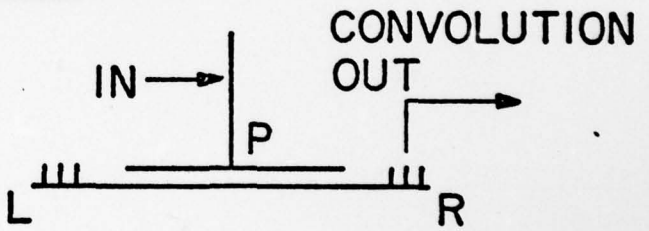
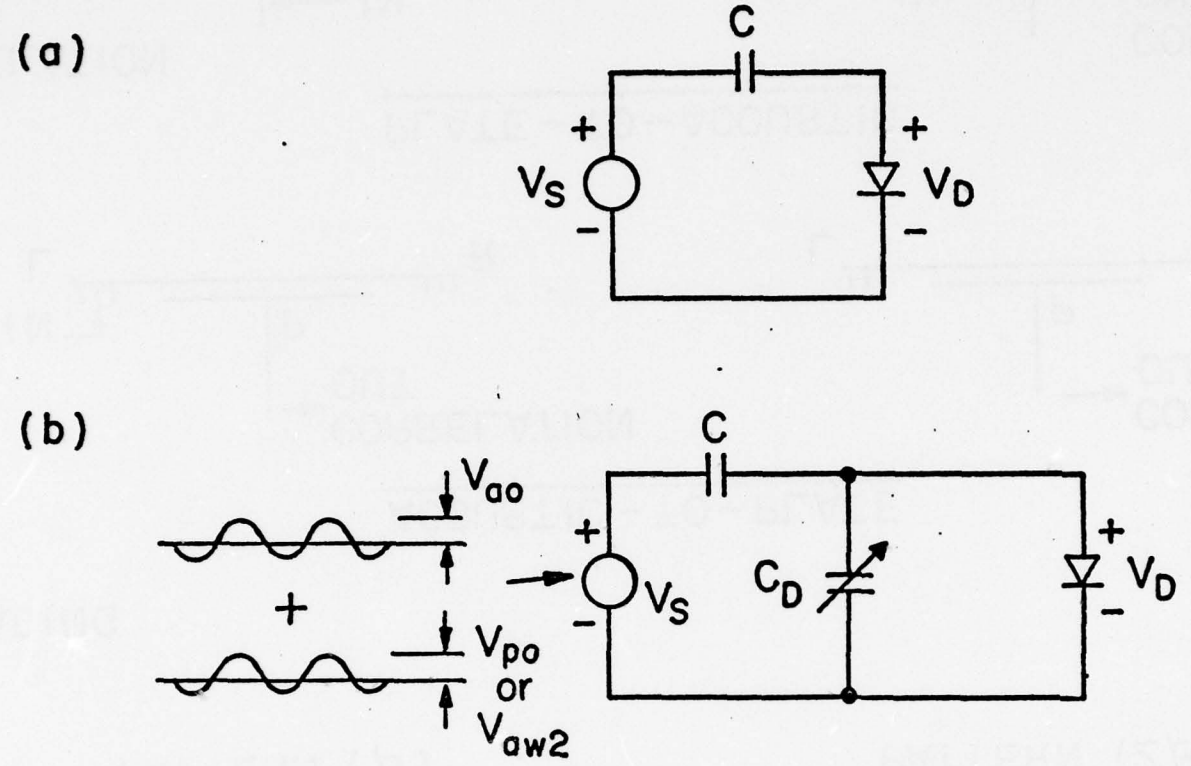


PLATE - TO - ACOUSTIC






(a)
C
+
V_S
−
+
V_D
−
(b)
V_{ao}
+
V_{po}
or
V_{aw2}
C
+
V_S
−
C_D
+
V_D
−

separating the acoustic surface wave from the diode array and the piezoelectric substrate sandwiched between the diode array and ground. The diode is a single element of the array. $V_s = V_a + V_p$ is a source composed of the sume of two voltage components. V_a is a low level component due to the surface wave potential, V_p is an externally applied plate signal that may be either a short duration high amplitude sampling pulse or a low level rf signal.

i) Acoustic-Plate Writing with a High Amplitude Plate Pulse

The plate pulse voltage V_p is assumed to be of sufficient amplitude to turn on the diode, so that it acts essentially like a closed switch. Thus, a charge $Q_s = CV_s = C(V_a + V_p)$ is deposited in the coupling capacitor, C . When the pulse turns off, the charged coupling capacitor C appears directly across the diode, reverse biasing it. The stored charge now leaks out of C slowly with the diode reverse leakage current.

The full diode array is next considered. Each diode is located at a position z_n and the sampling pulse is on at a time t_p , so that the stored charge pattern is of the form:

$$Q_s(z) = C\left(V_a e^{j(\omega t_p - \beta z_n)} + V_p\right)$$

where ω and β are the surface wave frequency and propagation constant, respectively. If there are at least two diodes per acoustic wavelength, and if the pulse duration is shorter than $2\pi/\omega$, then by the Nyquist sampling theorem enough samples are stored to reconstruct the surface wave modulation V_a and spacial phase, $e^{-j\beta z}$.

ii) Acoustic-Plate Writing with a Low Level RF Signal

The circuit model of Fig. 4(b) is appropriate for acoustic-plate writing when the plate signal is a low amplitude rf pulse. Now, the source voltage V_s is of the form:

$$V_s = V_a e^{j(\omega t - \beta z)} + V_p e^{j\omega t} \quad .$$

In this case, the acoustic potential V_a is usually the dominant component of V_s and neither V_a nor V_p is of sufficient amplitude to strongly turn on the diode. Thus, the diode current flows largely through the depletion layer capacitor C_D. The diode voltage V_D is of the form:

$$V_D = \frac{C}{C + C_D} V_s(t) - V_0$$

where V_0 is due to charge stored in the diode capacitance C_D.

Here, positive half cycles of the source voltage V_s weakly forward bias the diode so that it acts like a switch with a high series resistance. Now the charging process is drawn out over several cycles of V_s until sufficient current has flown to completely charge the coupling capacitor C.

The amplitude and phase of the stored charge pattern can be determined by noting that the surface wave potential samples the plate signal with successive peaks spaced in time by $2\pi/\omega$. The total stored charge Q_s is given by

$$Q_s = Q_0 + \sum_m K(t_p + 2m\pi/\omega)\, V_p(t_p + 2m\pi/\omega)\, e^{j(\phi_0 + \beta z_n + 2m\pi)}$$

$$= Q_0 + e^{j(\phi_0 + \beta z_n)} \sum_m K(t_p + 2m\pi/\omega)\, V_p(t_p + 2m\pi/\omega) \quad .$$

The charge Q_0 is a spacially uniform component of the total charge Q_s due to the surface wave alone scanning the diode array; t_p and ϕ_0 are the time and phase of the first surface wave peak, and $K(t)$ is a slowly varying factor. Thus, the stored charge pattern has a component that retains the surface wave spacial phase and a weighted sum — or integral, if m is large — of the plate signal modulation V_p .

iii) Acoustic-acoustic Writing

The two surface wave amplitudes are V_{a1} and V_{a2} and reference is again made to Fig. 4(b). The source voltage V_s is now of the form

$$V_s = V_{a1}e^{j(\omega t-\beta z)} + V_{a2}e^{j(\omega t+\beta z)} \quad .$$

For the case of $V_{a1} >> V_{a2}$, the analysis is identical to that of acoustic plate writing with a low level rf plate signal. Now, however,

$$Q_s = Q_0 + \sum_m K(t_p + 2m\pi/\omega)\, V_{a2}(t_p + 2m\pi/\omega)\, e^{j(\phi_0+2\beta z_n+2m\pi)}$$

$$= Q_0 + e^{j(\phi_0+2\beta z_n)} \sum_m K(t_p + 2m\pi/\omega)\, V_{a2}(t_p + 2m\pi/\omega) \quad ,$$

so that the spacially varying component of Q_s has twice the spacial phase of each surface wave.

iv) Storage

During the storage interval, charge resides in both the diode capacitor C_D and the parallel piezoelectric substrate capacitance C_p , as in Fig. 2(b). This charge is lost linearly in time with the diode reverse leakage current I_R , so that the stored charge $Q_s(t)$ is given by $Q_s(t) = Q_{s0} - I_R t$, where Q_{s0} is the original stored charge. The stored

charge may thus be scaled appropriately for any delay between writing and reading.

v) Reading

The readout process employs the varactor properties of the diodes. Thus, the circuit of Fig. 2(c) applies, where the source V_r is due to the surface wave potential in the acoustic-to-plate mode, or the externally applied rf signal in the plate-to-acoustic mode. A component of the diode voltage appears as the product of the reading signal voltage V_r and the stored charge Q_s. In acoustic-to-plate reading, this has the form of an rf voltage. The plate electrode on the back of the diode array sums the diode voltages over the array length, so that the output voltage is seen as

$$V_{out} \propto e^{j\omega t} \int_{array} Q_s(z/v)\, V_r(t \pm \tfrac{z}{v})\, d(z/v) \quad .$$

The sign of z/v in the argument of V_r depends on the choice of input transducer.

In the case of plate-to-acoustic reading, the readout component of the diode voltage is of the form $Q_s(z)e^{\pm j\beta z}\, V_r e^{\pm j\omega t} = Q_s V_r e^{\pm j(\omega t \pm \beta z)}$. This excites surface waves which propagate to both transducers. The amplitude of the surface wave propagating back toward the original input transducer has the form

$$V_{sw.} \propto e^{j(\omega t + \beta z)} \int_{array} V_r[t + (z/v_a)]\, Q_s(z/v)\, d(z/v) \quad ,$$

(correlation)

and toward the opposite transducer has the form

$$V_{sw} \propto e^{j(\omega t-\beta z)} \int_{\text{array}} V_r[t - (z/v_a)]\, Q_s(z/v_a)\, d(z/v) \quad \text{(convolution)} .$$

Thus in both readout modes the output appears as either the convolution or correlation of the stored charge pattern and the readout signal.

The analysis will be performed for both fast (such as Schottky) and p-n junction diodes. A fast diode is a device whose conduction current is of the form $I_s\left(e^{qV_D/mkT} - 1\right)$, regardless of the rise time of the diode voltage, V_D. This is seldom true for p-n diodes in this application. Hence, the analysis will account for their transient response.

The theory is readily adapted to either type of diode with conductive overlays. The results are analytic when the overlay is modeled as a fixed capacitor in parallel with the diode. This assumption is usually reasonable.

2. Writing

The analysis of the various modes of writing a charge pattern into the diode array follows. Writing with a single pulse is first considered for both fast and p-n junction diodes. Treatment of the low level input case then follows, again for both types of diodes.

i) Writing into Fast Diodes with a Single Pulse

The charging of an array of fast diodes with a single pulse is analyzed by adopting a complete circuit model that may be reduced with reasonable

simplifications. Analytic forms for the total stored charge and the component with the spacial periodicity of the surface wave are then found.

The complete circuit model in Fig. 5(a) is composed of two separate loops coupled through the diode. The left loop models the coupling of the electric fields associated with the traveling acoustic surface wave to the diode through a capacitor C_a given by [10]

$$C_a = \beta\epsilon_0 \left[\frac{\epsilon_0 + \epsilon_p \tanh(\beta h)}{(\epsilon_0 + \epsilon_p)[1 + \tanh(\beta h)]} \right] \left(\operatorname{sinc} \frac{\beta\delta}{2} \right) \qquad (1)$$

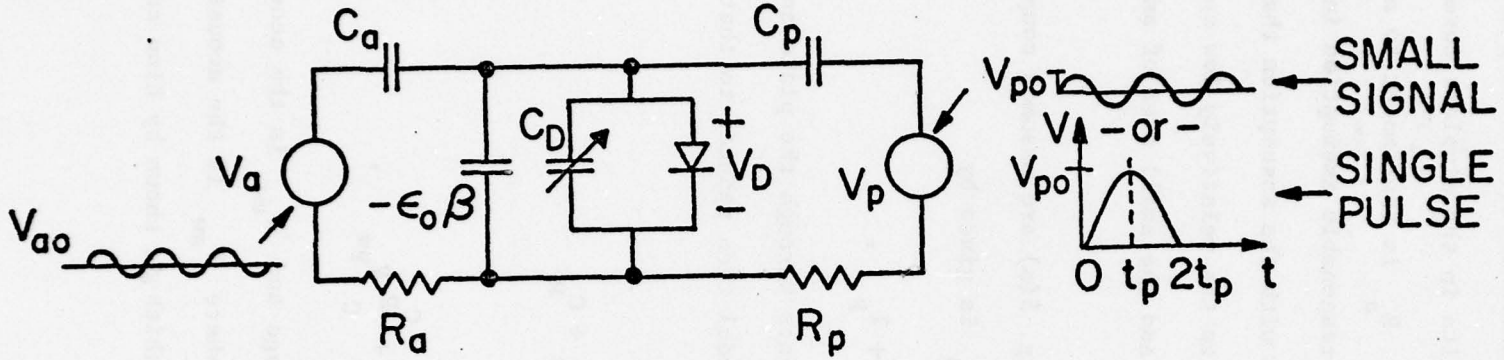
This form may be derived directly from the equations for the space charge field above the piezoelectric, as is done by Kino and Reeder Here, ϵ_0 is the dielectric constant of free space. ϵ_p is an effective dielectric constant for the piezoelectric, given by

$$\epsilon_p = (\epsilon_{yy}\epsilon_{zz} - \epsilon_{yz}^2)^{1/2} \quad . \qquad (2)$$

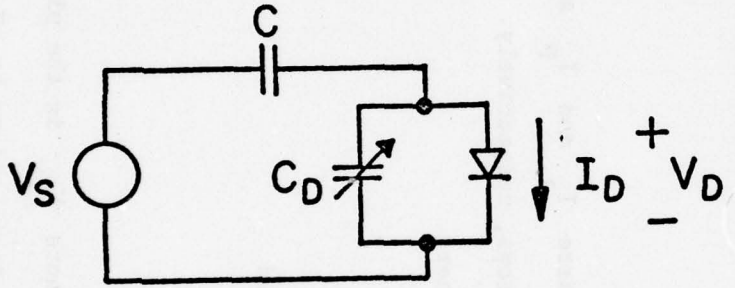
The stress free dielectric tensor, $\underline{\epsilon}^T$ is used; for YZ - $LiNbO_3$, $\epsilon_p = 50.2$. The $\operatorname{sinc}(\beta\delta/2)$ is due to field averaging over the diode width δ . This formulation for the acoustic circuit is valid when the perturbation due to the presence of the diode array is small, so that the principal propagating mode is a Rayleigh wave with propagation constant $\beta = \omega/v_a$, where ω is the frequency and v_a the propagation constant.

The negative capacity $-\epsilon_0\beta$ is usually negligible compared to the diode capacity, C_D , and will be henceforth ignored. R_a accounts for transverse currents between adjacent diodes. This may be shown to be the principal source of propagation loss due to the diode array.

(a) COMPLETE MODEL



(b) SIMPLIFIED MODEL



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The right loop models the coupling of plate signals to the diode. C_p is the capacity due to the piezoelectric substrate thickness d, and R_p arises from the source and semiconductor bulk impedances.

In order to obtain analytic results in the simplest form, we shall ignore both R_a and R_p. Dropping R_a is tantamount to assuming good isolation between adjacent diodes, a reasonable assumption in mesa and overlay diode arrays. R_p is ignored with the assumption that $R_p C_p \ll \omega/2\pi$. This, too, is nearly always true due to the relatively low spreading resistance of the semiconductor substrate and the small area of an element of the diode array.

The two loops of the model in Fig. 5(a) are assumed coupled only to the extent that the diode current I_D is given by

$$I_D = I_a + I_p \quad , \tag{3}$$

where I_a and I_p are the net currents through the plate and acoustic loops, respectively. The complete model then reduces to that of Fig. 5(b), where

$$C = C_a + C_p \tag{4}$$

and

$$V_s = \frac{C_a}{C} V_{aw} + \frac{C_p}{C} V_{pw} \quad , \tag{5}$$

where V_{pw} is the plate signal voltage and V_{aw} is the acoustic source voltage, given by $V_{aw} = \sqrt{2 Z_a P_{aw}}$, where P_{aw} is the acoustic power and Z_a is the acoustic impedance, which is shown by Kino and Reeder

to be

$$Z_a = \frac{2|\Delta v/v_a|\, e^{-2\beta h}}{\omega w(\epsilon_0 + \epsilon_p)} \quad . \tag{6}$$

The expression $|\Delta v/v_a|$ is the fractional change in Rayleigh surface wave velocity produced by a shorted surface and w is the acoustic beam width.

The fast diode model is composed of a current load

$$I_D = I_s\left(e^{qV_D/kT} - 1\right) \cong I_s e^{qV_D/kT} \tag{7}$$

in parallel with a depletion layer capacitor C_D . For our purpose, C_D is defined in terms of Q_D , the charge in the diode, given in the abrupt depletion layer approximation by

$$\begin{aligned} Q_D &= \sqrt{2qN_D\epsilon_s V_B} - \sqrt{2qN_D\epsilon_s (V_B - V_D)} \\ &= C_{D0}V_B - C_D(V_B - V_D) \end{aligned} \tag{8}$$

where

$$C_D = \sqrt{\frac{2qN_D\epsilon_s}{(V_B - V_D)}} \quad . \tag{9}$$

Here, I_s is the diode reverse saturation current, q is the electron charge, k is Boltzmann's constant, T is the temperature, N_D and ϵ_s are the semiconductor doping density and dielectric constant, V_B is the built-in junction potential, and C_{D0} is the diode capacitance when $V_D = 0$.

In the writing process, charge is stored due to the flow of diode conduction current, which increases exponentially with the diode voltage. We shall assume that only one of the two components of the source voltage V_s is of sufficient amplitude to cause a significant conduction current to flow. This signal will take the form of one or more sharply peaked pulses. Most diode conduction current will flow near the tip of each peak. Thus, the larger component of the source voltage V_s is used purely to control the current used to store charge.

The second, smaller component of the source voltage V_s is modulated by the phase and amplitude information to be stored. This signal by itself is too small to cause a significant diode conduction current to flow. It contributes to the current only when the larger signal is near a peak and conduction current is already flowing.

The circuit model of Fig. 5(a) includes the diode depletion layer capacitor C_D. For small values of source voltage V_s, the diode current is principally displacement current through this capacitor, and the diode voltage V_D varies nearly linearly with the source voltage V_s. For large V_s, the diode conduction current dominates and the diode voltage V_D saturates. Only in this saturation regime does sufficient current flow to completely charge the circuit with a single pulse. The turn-on voltage V_{on}, defining the minimum plate pulse voltage V_{p0} required for complete charging, is reached approximately when the charge in the coupling capacitor, $C(V_s - V_D)$, equals the diode charge evaluated at the diode saturation voltage.

The diode capacitance C_D varies with the diode voltage V_D as $C_D \sim (V_B - V_D)^{-1/2}$. It is not possible to include such a dependence in an analytic theory. Nevertheless, the diode capacitance C_D remains essentially constant for changes in diode voltage small compared to the built-in

voltage V_B . This constant C_D approximation is valid over certain regions of operation. During the peak of the charging pulse, we assume a value C_{Dp} , the diode capacitance evaluated at the peak level of diode voltage, V_{Dp} . For writing with small signals, the zero bias diode capacitance C_{DO} may be used. During storage and readout, the diode reverse bias voltage is used to evaluate C_D .

The current equation for the simplified model, Fig. 4(a), is

$$C \frac{d}{dt} (V_s - V_D) = \frac{dQ_D}{dt} + I_s e^{qV_D/kT} , \qquad (10)$$

where Q_D is the charge in the diode depletion layer capacitor C_D .

During charging, the diode charge Q_D is the sum of a rapidly varying component due to the source V_s and a slowly varying component due to the stored charge Q_s . Thus, the assumed solution to the charging equation is

$$Q_D(t) = C(V_s - V_D) - Q_s(t) . \qquad (11)$$

Substitution of (11) into (10) yields the explicit equation for the stored charge Q_s in terms of the source voltage V_s . This is done by writing the diode voltage V_D in terms of the diode charge Q_D with the aid of Eq. (8) and yields

$$\frac{dQ_s}{dt} = I_s \exp\left\{\frac{q}{kTC_T}\left[CV_s + (C_D - C_{DO})V_B - Q_s\right]\right\} \qquad (12)$$

where, for compactness, we write $C_T = C + C_D$.

Now consider the solution for Eq. (12) when a single sharply peaked plate pulse is used to store information contained in a low level acoustic

signal. The plate pulse V_p is assumed parabolic in shape, so that the source voltage V_s takes the form

$$V_s(t) = \frac{C_a}{C} V_{a0} \sin(\omega t - \beta z) + \frac{C_p}{C} V_{p0} \left[1 - \left(\frac{t - t_p}{t_p}\right)^2\right] , \qquad (13)$$

where t_p is the time at which the plate pulse voltage V_p reaches a peak. Solving (12) we assume a peak diode capacitance C_{Dp}, with $C_{Tp} = C + C_{Dp}$. The stored charge Q_s is then given by

$$Q_s = \frac{kT}{q} C_{Tp} \ln \left[\sqrt{\frac{\pi q}{kTV_{p0}CC_{Tp}}} I_s t_p \, e^{(q/kTC_T)[CV_s(t_p)+V_B(C_{Dp}-C_{D0})]} + 1 \right] \qquad (14)$$

For most cases of interest, the argument by the logarithm is much greater than unity, and

$$Q_s \approx CV_s(t_p) + V_B(C_{Dp} - C_{D0}) + \frac{kT}{q} C_{Tp} \ln \left[I_s t_p \sqrt{\frac{\pi q}{kTV_{p0}CC_{Tp}}} \right] , \qquad (15)$$

where

$$CV_s(t_p) = C_a V_{a0} \sin(\omega t_p - \beta z) + C_p V_{p0} . \qquad (16)$$

It is seen that the first term on the right hand side of Eq. (15) retains the modulation, V_{a0}, and spacial phase, βz, of the surface wave. It is this component of charge that gives rise to the readout — we shall name it the readout charge, $Q_R \sin(\omega t_p - \beta z)$ — given by

$$Q_R = C_a V_{a0} . \qquad (17)$$

From (15) and (8), the diode voltage is given by

$$V_D(t) = \frac{C}{C_T}[V_s - V_s(t_p)] + \frac{V_B}{C_T}(C_D - C_{Dp}) - \frac{kT}{q}\frac{C_{Tp}}{C_T}\ln\left[I_s t_p \sqrt{\frac{\pi q}{kTCC_{Tp}V_{p0}}}\right] \tag{18}$$

where C_D and $C_T = C_D + C$ are evaluated with the diode voltage V_D given by Eq. (18). The last term on the RHS of (18) gives the peak diode voltage, V_{Dp}, as

$$V_{Dp} = -\frac{kT}{q}\ln\left[I_s t_p \sqrt{\frac{\pi q}{kTCC_{Tp}V_{p0}}}\right] . \tag{19}$$

The diode reverse voltage is given by Eq. (18) with the source voltage $V_s = 0$. This is

$$V_D = -\left\{\frac{V_s(t_p)}{C_T} + \frac{V_B(C_{Dp} - C_D)}{C_T} + \frac{kT}{q}\frac{C_{Tp}}{C_T}\ln\left[I_s t_p \sqrt{\frac{\pi q}{kTCC_{Tp}V_{p0}}}\right]\right\} . \tag{20}$$

The turn-on voltage V_{on} is the plate voltage V_{p0} required to saturate the diode voltage. With the coupling capacitor charge $C(V_s - V_{Dp})$ set equal to the diode charge at the saturation voltage V_{Dp} [Eq. (19)], V_{on} is

$$V_{on} = \frac{C_a V_{a0}}{C_T} - \frac{kT}{q}\frac{C_{Tp}}{C_p}\ln\left[I_s t_p \sqrt{\frac{\pi q}{kTCC_{Tp}V_{p0}}}\right] + \frac{V_B}{C_p}(C_{D0} - C_{Dp}) . \tag{21}$$

ii) Writing Into p-n Junction Diodes with a Single Pulse

The transient response of p^+n junction diodes is now considered to show how the fast diode model must be modified for single pulse writing.

In Appendix A, the excess minority carrier charge density at the edge of the neutral region, $p_n(0,t)$, for times much shorter than the minority carrier lifetime was shown to be

$$p_n(0,t) = p_{n0}\left(e^{qV_D/kT} - 1\right) = \frac{1}{q\sqrt{\pi D_p}} \int_0^t \frac{I_D(\tau)}{(t-\tau)^{1/2}}\, d\tau \quad . \qquad (22)$$

By rewriting Eq. (22), the diode voltage is found to be

$$V_D(t) = \frac{kT}{q}\, \ell n \left[1 + \frac{1}{qp_{n0}\sqrt{\pi D_p}} \int_0^t \frac{I_D(\tau)}{(t-\tau)^{1/2}}\, d\tau\right] \quad . \qquad (23)$$

The analysis is completely parallel to the fast diode case, so that the simplified circuit model, Fig. 5(b), is appropriate. The source voltage V_s is again given by Eq. (13), where the dominant signal is a parabolic plate pulse peaking at a time t_p . We are here interested in the transient diode characteristics, which are in response to the sharply peaked plate pulse rather than the weaker acoustic signal.

Since the voltage drop is largely across the coupling capacitor C , the diode is driven by a linear current

$$I_D = C\frac{dV_s}{dt} \approx \frac{2CV_p}{t_p}\left[1 - (t/t_p)\right] \quad . \qquad (24)$$

Substitution of (24) into (23) gives the forward diode voltage V_D during charging,

$$V_D(t) = \frac{kT}{q}\, \ell n \left[1 + \frac{4CV_{p0}}{qP_{n0}t_p}\sqrt{t/\pi D_p}\left(1 - \frac{2}{3}\frac{t}{t_p}\right)\right] \quad . \qquad (25)$$

Typical values are $N_D = 5 \times 10^{14}/cm^3$ (10 Ω-cm), $C = 10^{-10}$ F/cm^2, $t_p = 2.5 \times 10^{-9}$ sec, $D_p = 20$ cm^2/sec, and $V_{p0} = 100$ volts. It is seen that V_D rapidly climbs to about 0.53 volts and remains essentially constant until $t \cong 3t_p/2$, when V_D rapidly drops to zero. At this time, $V_s = \frac{3}{4} V_{p0}$. For $t > 3t_p/2$, $V_D < 0$, and all diode conduction current ceases to flow. Thus, we expect the stored charge to be only 75% of that found in the fast diode case.

The rapid junction response is due to holes drifting across the depletion layer from the p^+ region to the n region. The p^+ region provides an essentially infinite reservoir of holes, and the speed of this process is limited by transit time across the depletion layer. Not all this charge will be stored, since insufficient time has elapsed to allow the holes to diffuse into the neutral region. The holes near the edge of the neutral region will drift back to the p^+ region when the diode current changes sign, at time $t > t_p$. This gives rise to a large diode reverse current during the time interval $t_p < t < \frac{3}{2} t_p$, during which 25% of the stored charge is lost. For times beyond $\frac{3}{2} t_p$, essentially no conduction current flows, resulting in the retention of the remaining 75% of the original stored charge.

Thus, p-n junction diodes act very much like fast diodes in this application, turning on rapidly and reaching nearly the same peak forward bias voltage. The only significant difference is that the readout charge for the p-n junction diode is given by

$$Q_R^{pn} = 0.75\, Q_R^{fast} \quad . \tag{26}$$

iii) Writing Into Fast Diodes with Low Level RF Signals

Plate-acoustic writing, $V_{p0} << V_{a0}$. This case is physically analogous to single pulse writing, except that the diode is never strongly forward biased. Thus, the diode forward current is low and several pulses are required to completely charge the circuit. The stored charge and diode voltage are found, as before, with the differential equation (13), except that the source voltage is given by

$$V_s(t) = \frac{C_a V_{a0}}{C} \sin(\omega t - \beta z) + \frac{C_p V_{p0}}{C} \sin \omega t \qquad (27)$$

with the assumptions that $e^{qV_{a0}/kT} >> e^{qV_{p0}/kT}$ and V_{a0} is of sufficiently low amplitude so that the diode displacement current greatly exceeds its conduction current. Reference is made to the equivalent circuit model of Fig. 3(b).

Because the diode is weakly forward biased, a constant zero bias diode capacitance $C_D = C_{D0}$ is assumed. The stored charge is then given by

$$Q_s = \frac{kT}{q} C_T \ln\left\{1 + \frac{qI_s}{kTC_T} \int_0^t \exp\left[\frac{q}{kTC_T}\left(C_a V_{a0} \sin(\omega t - \beta z) + C_p V_{p0} \sin \omega t\right)\right] dt\right\} \qquad (28)$$

The argument of the integral in (28) is sharply peaked when $\omega t - \beta z = \pi/2$. Thus, the integral is rewritten as

$$\frac{2\pi}{\omega} \exp\left[\frac{q}{kT} \frac{C_p}{C_T} V_{p0} \cos \beta z\right] \left\{\frac{N}{2\pi} \int_0^{2\pi} \exp\left(\frac{q}{kT} \frac{C_a}{C_T} V_{a0} \sin(\omega t - \beta z)\right) d(\omega t)\right\}$$

The integral is now recognized to be the zeroth order modified Bessel function of the first kind,

$$I_0\left(\frac{q}{kT}\frac{C_a}{C_T}V_{a0}\right) ,$$

where N is the number of rf cycles used for charging, $N = \omega t/2\pi$. Thus, (28) is written as

$$Q_s(t) = \frac{kT}{q} C_T \ln\left[1 + \frac{qI_s t}{kTC_T} I_0\left(\frac{q}{kT}\frac{C_a}{C_T} V_{a0}\right) \exp\left(\frac{q}{kT}\frac{C_p}{C_T} V_{p0} \cos \beta z\right)\right] \tag{29}$$

The diode voltage after charging, is given by

$$V_D \approx -\frac{Q_s}{C_T} = -\frac{kT}{q} \ln\left[1 + \frac{qI_s t}{kTC_T} I_0\left(\frac{q}{kT}\frac{C_a}{C_T} V_{a0}\right) \times \exp\left(\frac{q}{kT}\frac{C_p}{C_T} V_{p0} \cos \beta z\right)\right] . \tag{30}$$

The readout charge is the component of the stored charge Q_s with periodicity $\cos \beta z$. This is found by Fourier expansion of (29) to be

$$Q_R = \frac{kT}{\pi q} C_T \int_0^{2\pi} \cos\theta \ln\left[1 + \frac{qI_s t}{kTC_T} I_0\left(\frac{q}{kT}\frac{C_a}{C_T} V_{a0}\right) \times \exp\left(\frac{q}{kT}\frac{C_p}{C_T} V_{p0} \cos\theta\right)\right] d\theta . \tag{31}$$

The integral (31) is not easily tractable. For large t, it has an asymptotic form of

$$Q_R = C_p V_{p0} \tag{32}$$

For shorter times, the readout charge Q_R is of the form

$$Q_R \cong 2I_s t\, I_0\left(\frac{q}{kT} V_{a0} \frac{C}{C_T}\right) I_1\left(\frac{q}{kT} V_{p0} \frac{C}{C_T}\right) \tag{33}$$

where $I_1(x) = \frac{d}{dx}[I_0(x)]$.

Acoustic-acoustic writing ($V_{a1} >> V_{a2}$). For the case of writing with two acoustic signals, $V_{a1}e^{j(\omega t-\beta z)}$ and $V_{a2}e^{j(\omega t+\beta z)}$, with $e^{qV_{a1}/kT} >> e^{qV_{a2}/kT}$, the analysis follows with V_{a2} replacing V_{p0}. Now the readout charge Q_R is the component of the stored charge Q_s with spacial frequency $2\beta z$.

iv) Writing Into p-n Diodes with Low Level RF Signals

This case is analogous to that of the fast diode. The circuit model of Fig. 4(b) is appropriate, with the source voltage V_s given by Eq. (27) with the earlier assumptions applying. It will now be convenient to assume that the diode voltage is determined by the capacitive voltage divider of the coupling capacitor C and the diode capacitor C_D. Including a term due to the stored charge Q_s and assuming the diode capacity C_D remains constant at its zero bias value C_{D0}, the diode voltage is

$$V_D(t) = \frac{C}{C_T} V_s - \frac{Q_s}{C_T} \quad . \tag{34}$$

We apply Eq. (A-4) which allows calculation of the increment in minority carrier charge, ΔQ_p , during one rf cycle of the source voltage V_s . Since the current from the p^+ to n regions is due to minority carriers, this yields the increment in stored charge. Substituting (34) into (A-4) gives

$$\Delta Q_p = qp_{n0}\sqrt{D_p/\pi}\int_0^{2\pi}\frac{e^{(q/kTC_T)[CV_s(\tau)-Q_s]}}{(t-\tau)^{1/2}}\,d\tau \quad . \qquad (35)$$

If the increment in charge ΔQ_p is small so that charging occurs over a large number of rf cycles, then Eq. (35) may be written in the form of a differential equation,

$$\frac{dQ_s}{dt} \simeq \frac{\omega}{2\pi}\Delta Q = \frac{\omega q p_{n0}}{2\pi}\sqrt{D_p/\pi}\, e^{-(qQ_s/kTC_T)}\int_0^{2\pi} \times \frac{e^{(qC/kTC_T)V_s(\tau)}}{(t-\tau)^{1/2}}\,d\tau \qquad (36)$$

Integration of Eq. (36) gives the stored charge Q_s as

$$Q_s(t) = \frac{kT}{q}C_T\,\ell n\left[1+\frac{q}{kTC_T}\left(\frac{qp_{n0}}{\pi}\sqrt{\frac{2\omega D_p}{3}}\right)tI_0\left(\frac{qC_a}{kTC_T}V_{a0}\right) \times \exp\left(\frac{q}{kT}\frac{C_p}{C_T}V_{p0}\cos\beta z\right)\right] \quad . \qquad (37)$$

This result is identical to that for the fast diode with a saturation current I_s of

$$I_s = \frac{qp_{n0}}{\pi}\sqrt{2\omega D_p/3} \quad . \qquad (38)$$

Thus, the fast diode model holds for p-n junction diodes when I_s is used as given by Eq. (38). For a typical value of $N_D = 4.6 \times 10^{14}/cm^3$, $P_{n0} = 5.6 \times 10^5/cm^3$ with $\omega = 6.28 \times 10^8$ sec^{-1}, $D_p = 20$ cm^2/sec, we find $I_s = 2.6 \times 10^{-9}$ amps/cm^2. This is about 100 times smaller than the I_s for a PtSi Schottky diode.

v) The Effect of Conductive Overlays

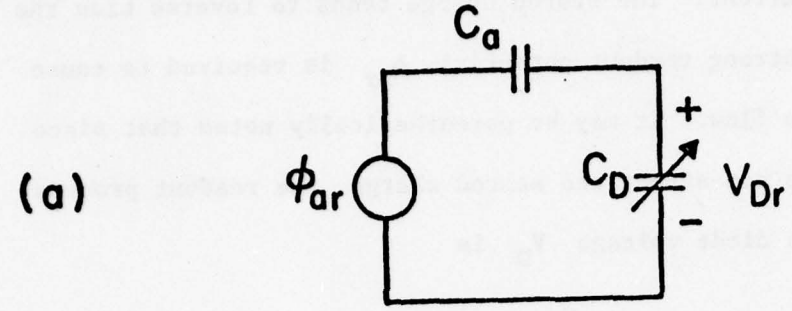
An overlay may be modelled as a capacitance in parallel with the diode depletion layer capacitor. This will not change the qualitative form of the above results, since the overlay can only increase the diode capacity.

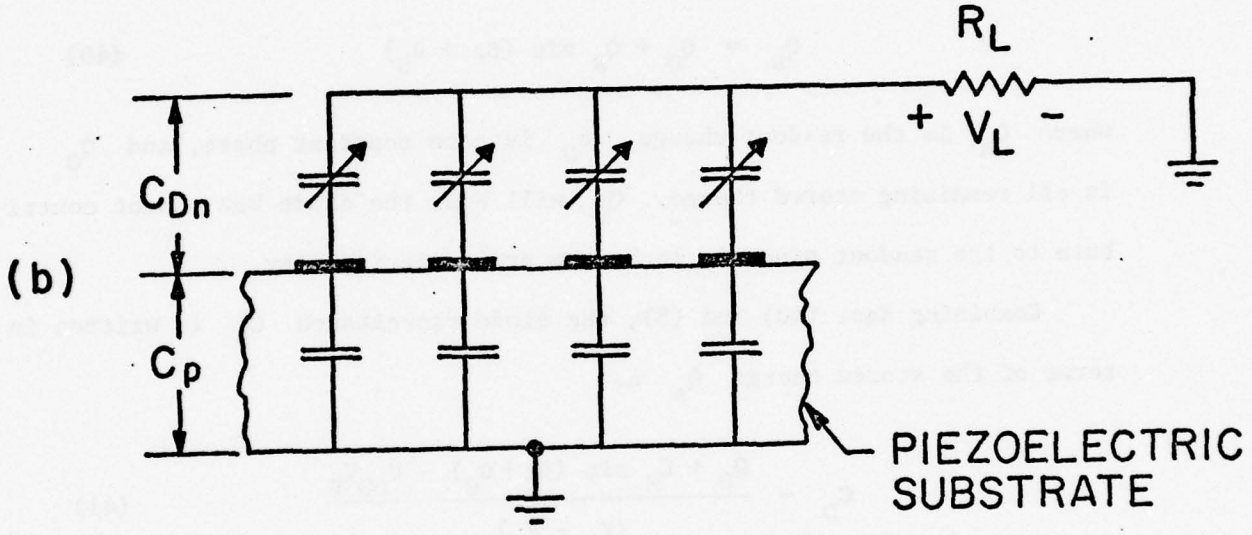
3. Reading

The various modes for reading the stored charge pattern are now considered. In all cases, the analysis finds the device output power in terms of the readout signal amplitude and the readout charge Q_R. We first deal with acoustic-to-plate reading, where the output appears at the plate in response to an acoustic readout signal. We then analyze plate-to-acoustic reading, where the output appears at one of the acoustic ports in response to an rf plate readout signal. Finally, the analysis of both readout modes is modified for the case of overlay diodes.

i) Acoustic-to-plate Readout

Here the readout signal is a surface wave propagating under the diode array and the output power is measured across a load resistor connected to the plate. The circuit model used to calculate the coupling of the surface wave potential ϕ_{ar} to the diode surface is seen in Fig. 6(a). Here, $\phi_{ar} = \sqrt{2P_{ar}Z_a}$, where P_{ar} is the readout surface wave power.


(a)
C_a
ϕ_{ar}
C_D
+
−
V_{Dr}


(b)
R_L
+ V_L −
C_{Dn}
C_p
PIEZOELECTRIC
SUBSTRATE

We have already used a similar model to calculate the surface wave coupling to the diode during writing. Now, however, we completely neglect the diode conduction current. The stored charge tends to reverse bias the diode, so that a very strong readout potential ϕ_{ar} is required to cause a conduction current to flow. It may be parenthetically noted that since the readout signal does not affect the stored charge, the readout process is nondestructive. The diode voltage V_D is

$$V_D = \frac{C_a}{C_a + C_D} \phi_{ar} \tag{39}$$

The total diode charge Q_s may be written as

$$Q_s = Q_0 + Q_R \sin(\beta z + \theta_0) \tag{40}$$

where Q_R is the readout charge, θ_0 is some constant phase, and Q_0 is all remaining stored charge. Q_0 will bias the diode but cannot contribute to the readout since it lacks the proper periodicity.

Combining Eqs. (40) and (8), the diode capacitance C_D is written in terms of the stored charge Q_s as

$$C_D = \frac{Q_0 + Q_R \sin(\beta z + \theta_0) - C_{D0} V_B}{(V_D - V_B)} \tag{41}$$

Substituting (41) into (39) and expanding, assuming $Q_R/(V_D - V_B)$ is small compared to the other terms, yields the component of diode voltage due to the product $Q_R \sin(\beta z + \theta_0) \times \phi_{ar}$, V_{Dr}, to be

$$V_{Dr} = \frac{C_a}{(C_a + C_D)^2} \frac{\phi_{ar} Q_R \sin(\beta z + \theta_0)}{(V_D - V_B)} \quad . \tag{42}$$

ϕ_{ar} varies as $e^{j(\omega t-\beta z)}$, so that a component of the diode reading voltage V_{Dr} appears as an rf potential with $\beta = 0$.

The voltage developed across each diode couples to the external load resistor R_L through the plate circuit coupling capacitor C_p , as shown in Fig. 6(b). The current through the n^{th} element of the diode array, I_n , is

$$I_n = C_p \frac{d}{dt}(V_{Drn} - V_L) = j\omega C_p (V_{Drn} - V_L) \tag{43}$$

where V_{Drn} is the voltage drop across the n^{th} diode and V_L is the voltage drop across the load resistor R_L . Thus, V_L is given by

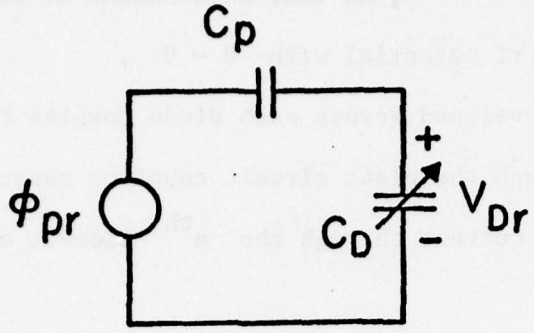
$$V_L = R_L \sum_n I_n = \frac{j\omega R_L C_p w\delta}{1 + j\omega NLR_L C_p w\delta} \sum V_{Dr}(Z_n) \tag{44}$$

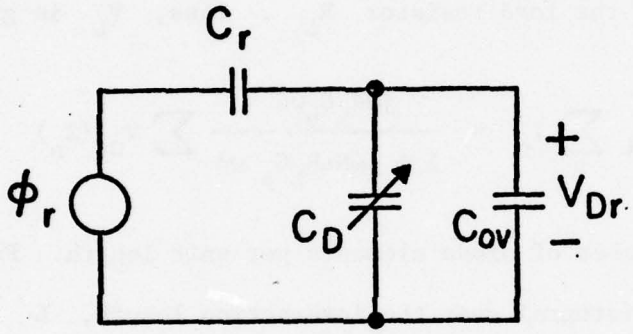
where N is the number of diode elements per unit length. For N large, the sum goes to an integral over the interaction length, L . This takes the form of the correlation or convolution of the stored charge pattern and the readout signal amplitude. In the simplest case, where both signals are of constant amplitude, the device output power, P_0 , is

$$P_0 = \frac{V_0^2}{2R_L} = \frac{1}{4R_L}\left[\frac{(\omega NLC_p R_L w\delta)^2}{1 + (\omega NLC_p R_L w\delta)^2}\right]\left[\frac{C_a}{(C_a + C_D)^2}\frac{Q_R \phi_{ar}}{(V_B - V_D)}\right]^2 \tag{45}$$

ii) Plate-to-acoustic Reading

We next consider plate-to-acoustic reading. Reference is made to the equivalent circuit model in Fig. 7. We first find the potential at the diode





READING MODE	ϕ_r =	C_r =
ACOUSTIC – TO – PLATE	ϕ_{ar}	C_a
PLATE – TO – ACOUSTIC	ϕ_{pr}	C_p

surface due to an applied plate reading signal. This potential excites a surface wave, whose amplitude may be calculated to obtain the device output power.

The diode voltage V_D appears across the capacitive voltage divider of the diode capacitance C_D and the capacity due to the piezoelectric substrate, C_p. For $C_p \ll C_D$,

$$V_D \approx \frac{C_p}{C_D} \phi_{pr} \quad , \tag{46}$$

where ϕ_{pr} is the amplitude of the externally applied plate readout signal. From Eqs. (8) and (9), the diode stored charge Q_s is written in the form

$$Q_s = Q_0 + Q_a = \frac{C_{DO}^2 V_B}{C_D} - C_{DO} V_B \quad . \tag{47}$$

We are primarily interested in the component of the diode surface potential that varies as $\cos(\omega t \pm \beta z)$. This corresponds to the first space harmonic component of the potential of the excited surface wave as seen at the surface of the diode. This potential, $V_{Dr}^{\pm}$, is

$$V_{Dr}^{\pm} = \frac{C_p}{2C_{DO}^2 V_B} \phi_{ar} Q_R \cos(\omega t \pm \beta z_n) \operatorname{sinc} \frac{\beta\delta}{2} \quad , \tag{48}$$

where z_n is the position of the n^{th} diode. The term $\operatorname{sinc}(\beta\delta/2)$ is due to the averaging of the potential over the finite diode width δ. The $\pm$ in the argument of the cosine arises because both forward (-) and backward (+) surface waves are excited.

The amplitude of the surface wave excited by the diode surface potential $V_{Dr}^{\pm}$ is found using the normal mode theory of Kino and Auld [ ]. From

Eq. (31) of this reference it may be shown that

$$\frac{\partial a}{\partial z} + j\beta^* = \frac{j\omega\rho_s\phi_1^* w}{4P_1} \qquad (49)$$

where w is the acoustic beam width, ρ_s is the semiconductor surface charge, and the rf potential due to the propagating acoustic wave is $\phi_a = a\phi_1$ where $P_1 = \phi_1^*\phi_1/2Z_a$. P_1 is the power per unit width of the surface wave and Z_a the acoustic impedance, is defined in Eq. (4).

The total rf potential is $\phi = \phi_a + \phi_s$, where ϕ_s is the sum of the contributions other than the fundamental acoustic surface wave mode. Kino and Reeder [11] define the relationship between ϕ_s, ρ_s , and the acoustic coupling capacitor C_a as

$$\phi_s = \rho_s/C_a \quad . \qquad (50)$$

Equation (49) now reduces to

$$\frac{\partial\phi_a}{\partial z} + j(\beta + \gamma)\phi_a = j\gamma\phi \quad , \qquad (51)$$

where

$$\gamma = \frac{\omega w C_a Z_a}{2} \qquad (52)$$

represents the perturbation on the surface wave propagation constant β due to the presence of the diode array. Assuming a solution

$$\phi_a(z) = \phi_a e^{+j(\beta+\gamma)(z'+z)} \quad ,$$

Eq. (42) may be integrated to give the potential of the fundamental acoustic mode:

$$\phi_a(z,\omega) = j\gamma \int \phi \, e^{j(\beta+\gamma)(z'+z)} \, dz' \quad . \tag{53}$$

By Fourier transforming Eq. (53), assuming the propagation constant $(\beta+\gamma)$ is constant in frequency. The potential ϕ_a as a function of time is seen to be

$$\phi_a(z,t) = j\gamma \int \phi\left(z', t - \frac{z'+z}{v_a}\right) e^{j\gamma z'} \, dz' \quad . \tag{54}$$

$V_{Da}^{\pm}$, the potential at the surface of each diode element, is not continuous. By using Floquet's theorem, $V_{Dr}^{\pm}(z_n)$ can be written in the form

$$V_{Dr}^{\pm}(z_n) = e^{-j\beta z} \, V(z) \quad , \tag{55}$$

where

$$V(z) = (\delta/\ell) V_{Dr0} \sum_{n=-\infty}^{\infty} \sin\left(\frac{\pi n \delta}{\ell}\right) e^{j(2\pi n/\ell)[z+(\delta/\ell)]} \tag{56}$$

δ/ℓ is the ratio of diode element width to the periodicity of the diode array. Retaining only the $n = 0$ term of (45) yields the result

$$V_{Dr}^{\pm}(z,t) = \phi(z,t) = (\delta/\ell) V_{Dr0} \, e^{-j\beta z} \, e^{\pm j\omega t} \quad . \tag{57}$$

If it is assumed that the original acoustic surface wave was perturbed by the presence of the semiconductor, so that its wavenumber was $\beta + \gamma$,

Eq. (54) yields the potential of the excited acoustic surface wave:

$$\phi_a = j\gamma e^{-j\gamma z} (\delta/\ell) \int V_{Dr0} e^{j(\omega t-\beta z)} dz' = j\gamma(\delta/\ell) V_{Dr0} L e^{-j\gamma z} e^{j(\omega t-\beta z)} \tag{58}$$

The output power is $\frac{\phi_a^* \phi_a}{2Z_a}$, so that combining Eqs. (58) and (39) yields the device output power P_0 for a constant amplitude rf plate readout signal ϕ_{pr} and stored readout charge Q_R, with a diode array length L:

$$P_0 = \frac{1}{2Z_a} \left[\frac{\gamma L \delta}{\ell}\right]^2 \left[\frac{C_p \phi_{pr} Q_R}{2C_{D0}^2 V_B} \operatorname{sinc} \frac{\beta\delta}{2}\right]^2 \tag{59}$$

iii) Reading With Overlay Diodes

Finally, we consider the effect of conductive overlays on the above results. Overlays are in general used to increase the effective area of the diodes by making ohmic contact to the diodes while covering, and hence shielding, a large part of the adjacent semiconductor area. They are insulated from the semiconductor bulk by a thin layer of SiO_2, thereby adding a large MOS capacitor in parallel with C_D. Thermally oxidized Si is usually accumulated at the surface, so that the typical flatband voltage shift $\sim$ 1.5 volts causes the MOS overlay capacitance to nearly equal the SiO_2 capacitance for most levels of reading signals. If this is not the case, the overlay itself will contribute to the readout signal, and analytic results are not easily obtained.

Changes in the readout analysis arise because most of the stored charge resides in the static overlay capacitor, where it cannot contribute to the readout. A single circuit model, shown in Fig. 8, is applicable to both plate and acoustic readout. Here, the capacitor C_r and reading signal ϕ_r represent C_p and ϕ_{pr} for plate-to-acoustic reading, and C_a and ϕ_{ar} for acoustic-to-plate reading. In both cases, $C_{ov} + C_D >> C_r$, where C_{ov} is the overlay capacity, so that the diode voltage is

$$V_D \approx \frac{C_r}{C_{ov} + C_D} \phi_r \approx \frac{C_r}{C_{ov}} \left(1 + \frac{C_D}{C_{ov}}\right) \phi_r \qquad (60)$$

The fraction of the readout charge Q_R residing in the diode capacity C_D, Q_{RD}, is

$$Q_{RD} = \frac{A}{A_D} \left[\frac{C_D(V_D - V_B) + C_{DO}V_B}{C_{ov}V_D}\right] Q_R \quad , \qquad (61)$$

where A is the overlay area and A_D is the diode area. Substituting the diode capacitance C_D in the form of Eq. (41) gives V_{Dr}, the component of diode voltage contributing to the readout

$$V_{Dr} = \frac{C_r[C_D(V_D - V_B) + C_{DO}V_B]}{C_{ov}^3 V_D(V_D - V_B)} Q_R \phi_r \quad . \qquad (62)$$

Combining (51) with the earlier analysis yields, the output power for acoustic-to-plate reading is

$$P_0 = \frac{1}{4R_L} \left[\frac{(\omega N L C_p R_L w \delta)^2}{1 + (\omega N L C_p R_L w \delta)^2}\right] \left[\frac{C_a[C_D(V_D - V_B) + C_{DO}V_B]}{C_{ov}^3 V_D(V_D - V_B)} Q_R \phi_{ar}\right]^2 \qquad (63)$$

The output power for plate-to-acoustic reading is:

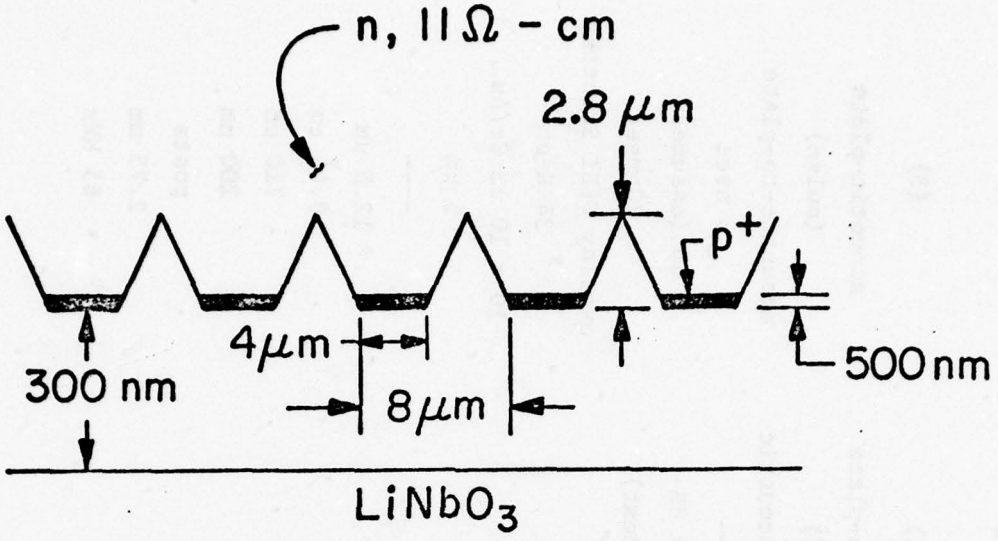
$$P_0 = \frac{1}{2Z_a}\left[\frac{\gamma L\delta}{\ell}\right]^2\left[\frac{C_p[C_D(V_D-V_B)+C_{DO}V_B]}{C_{ov}^3 V_D(V_D-V_B)}\,Q_R\phi_{pr}\,\mathrm{sinc}\,\frac{\beta\delta}{2}\right]^2 \qquad (64)$$

4. Comparison to Experiment

We now consider experimental verification of the theory. Table II summarizes the various writing and reading modes and device structures used in the experiments. The p^+n junction diode results were obtained in our own laboratory. The Schottky diode results have been previously reported by Ingebrigtsen [ ].

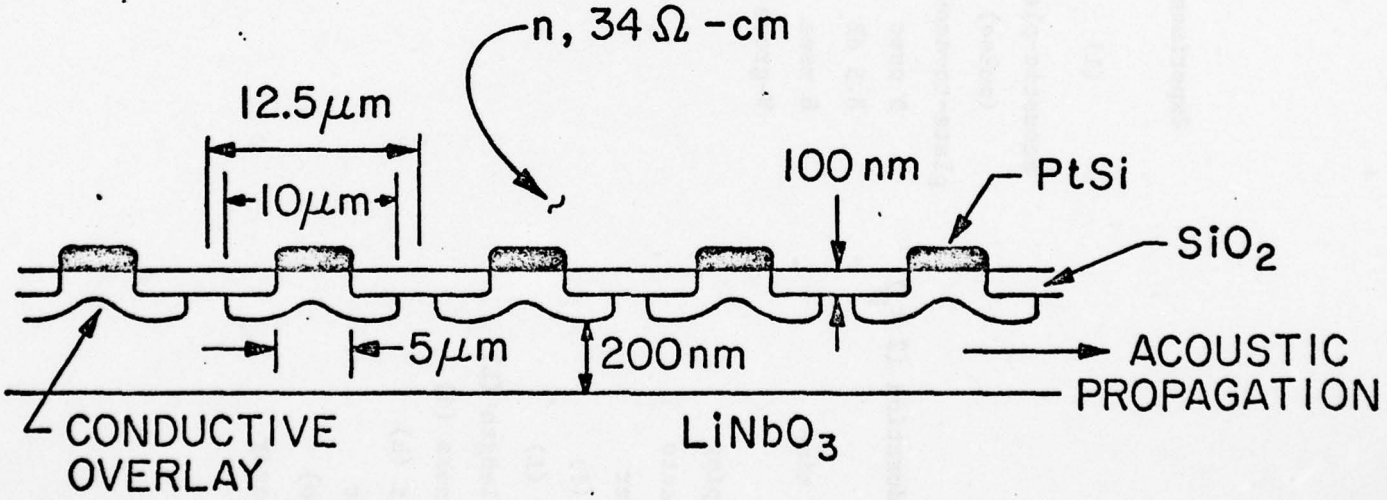
Figure 9 shows the two diode structures; in both cases interactions from the interdiode region are minimized. In the mesa structure of Fig. 9(a), this region has simply been etched away. Such a structure also provides excellent isolation between adjacent diodes.

The conductive overlays, shown in Fig. 9(b), shield the interdiode region from surface wave fields. As discussed earlier, such overlays put a large MOS capacitor in parallel with the diode. When the silicon surface is accumulated, this capacitor is static and does not contribute to writing or reading. The flatband voltage shift for the particular device discussed here is $\sim$ 1.5 volts [ ]. Thus, the overlay capacitor is always static in writing, and only contributes to readout for high levels of either the readout signal or reverse bias diode voltage due to the stored charge.



V GROOVE MESA p^+n DIODES

(a)



PtSi OVERLAY DIODES

(b)

TABLE II

Experimental Device Parameters

	(1)	(2)	(3)
Writing:	acoustic-plate (pulse)	acoustic-plate (rf)	acoustic-plate (pulse)
Reading:	plate-to-acoustic	plate-to-acoustic	acoustic-to-plate
Plate pulse duration ($2\tau_p$)	5 nsec	---	5 nsec
One way loss	8.5 dB	10.5 dB	8 dB (assumed)
3 dB storage time	8 msec	(see text)	∿ 20 msec
Diodes	V-grove isolated mesa p^+n		overlay PtSi Schottky
Substrate doping	∿ 11 Ω-cm		34 Ω-cm
Overlay contacts	----		10 × 10 μm Cr/Au
Diode diameter	----		5 μm
Diode width (δ)	4 μm		----
Diode period (ℓ)	8 μm		12.5 μm
Interaction length (L)	1.57 cm		0.44 cm
$LiNbO_3$ thickness (d)	450 μm		710 μm
Airgap height (h)	300 nm		200 nm
Airgap spacer	rails		posts
Beam width (w)	1 mm		2.75 mm
Center frequency	108 MHz		65 MHz

1) p^+n Junction Diodes, Acoustic-Plate Writing with a Single Pulse, Plate-to-Acoustic Reading

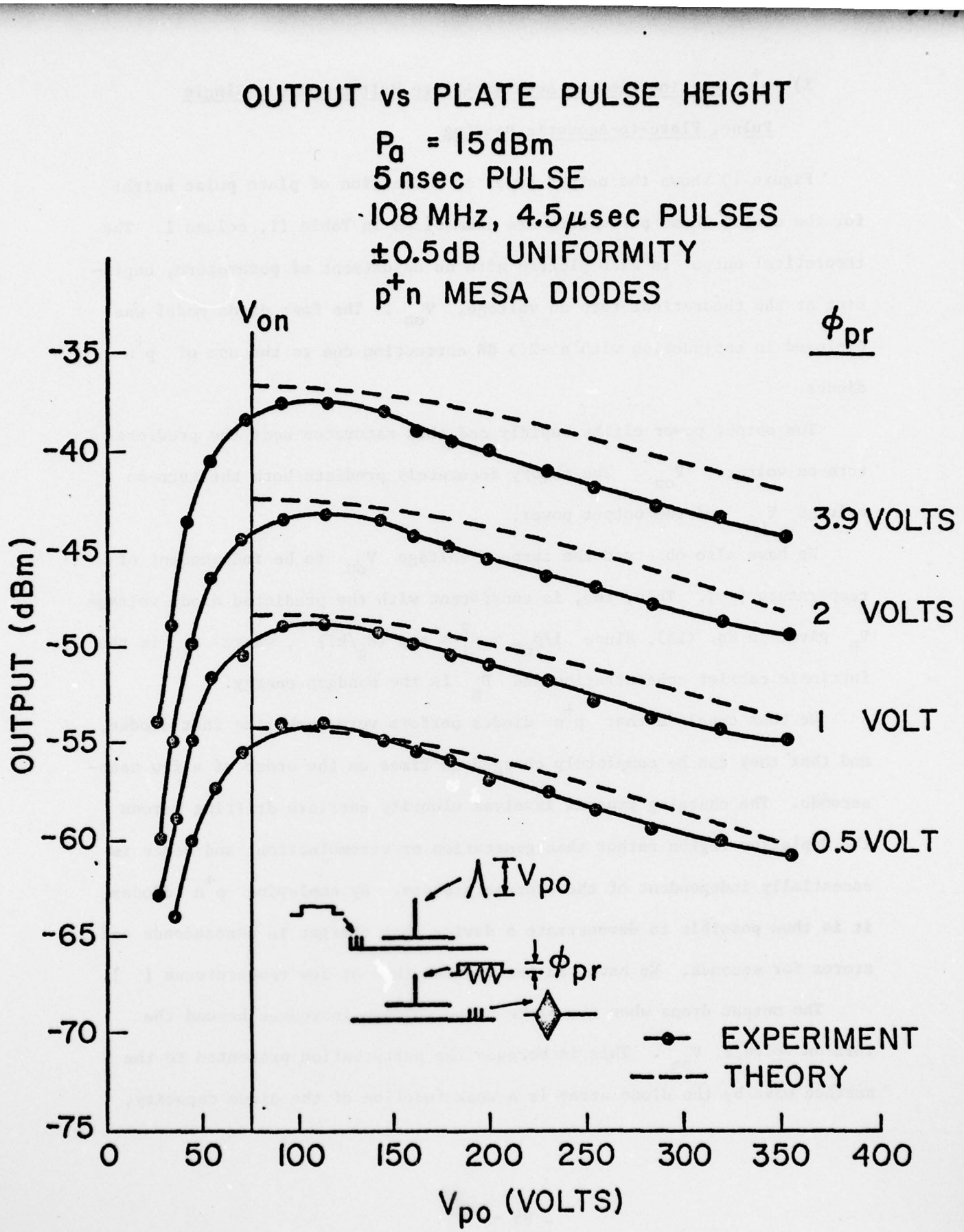
Figure 10 shows the output power as a function of plate pulse height for the device whose parameters are summarized in Table II, column 1. The theoretical output is also plotted with no adjustment of parameters, beginning at the theoretical turn-on voltage, V_{on}. The fast diode model was employed in conjunction with a -2.5 dB correction due to the use of p^+n diodes.

The output power climbs rapidly and then saturates near the predicted turn-on voltage, V_{on}. The theory accurately predicts both the turn-on voltage V_{on} and the output power.

We have also observed the turn-on voltage V_{on} to be independent of temperature [ ]. This, too, is consistent with the predicted diode voltage V_D given in Eq. (25), since $1/p_{n0} \sim n_i^2 \sim \exp(E_g/kT)$, where n_i is the intrinsic carrier concentration and E_g is the bandgap energy.

We thus conclude that p^+n diodes perform very much like fast diodes, and that they can be completely charged in times on the order of a few nanoseconds. The charging process involves minority carriers drifting across the depletion region rather than generation or recombination, and hence is essentially independent of the storage process. By employing p^+n diodes, it is thus possible to demonstrate a device that charges in nanoseconds and stores for seconds. We have, in fact, shown this at low temperatures [ ].

The output drops when the plate pulse voltage increases beyond the turn-on voltage V_{on}. This is because the perturbation presented to the surface wave by the diode array is a weak function of the diode capacity,


OUTPUT vs PLATE PULSE HEIGHT
P_a = 15dBm
5nsec PULSE
108 MHz, 4.5μsec PULSES
±0.5dB UNIFORMITY
p^+n MESA DIODES
V_{on}
ϕ_{pr}
3.9 VOLTS
2 VOLTS
1 VOLT
0.5 VOLT
OUTPUT (dBm)
-35
-40
-45
-50
-55
-60
-65
-70
-75
0
50
100
150
200
250
300
350
400
V_{po} (VOLTS)
$\Delta I V_{po}$
$\frac{1}{T}\phi_{pr}$
EXPERIMENT
THEORY

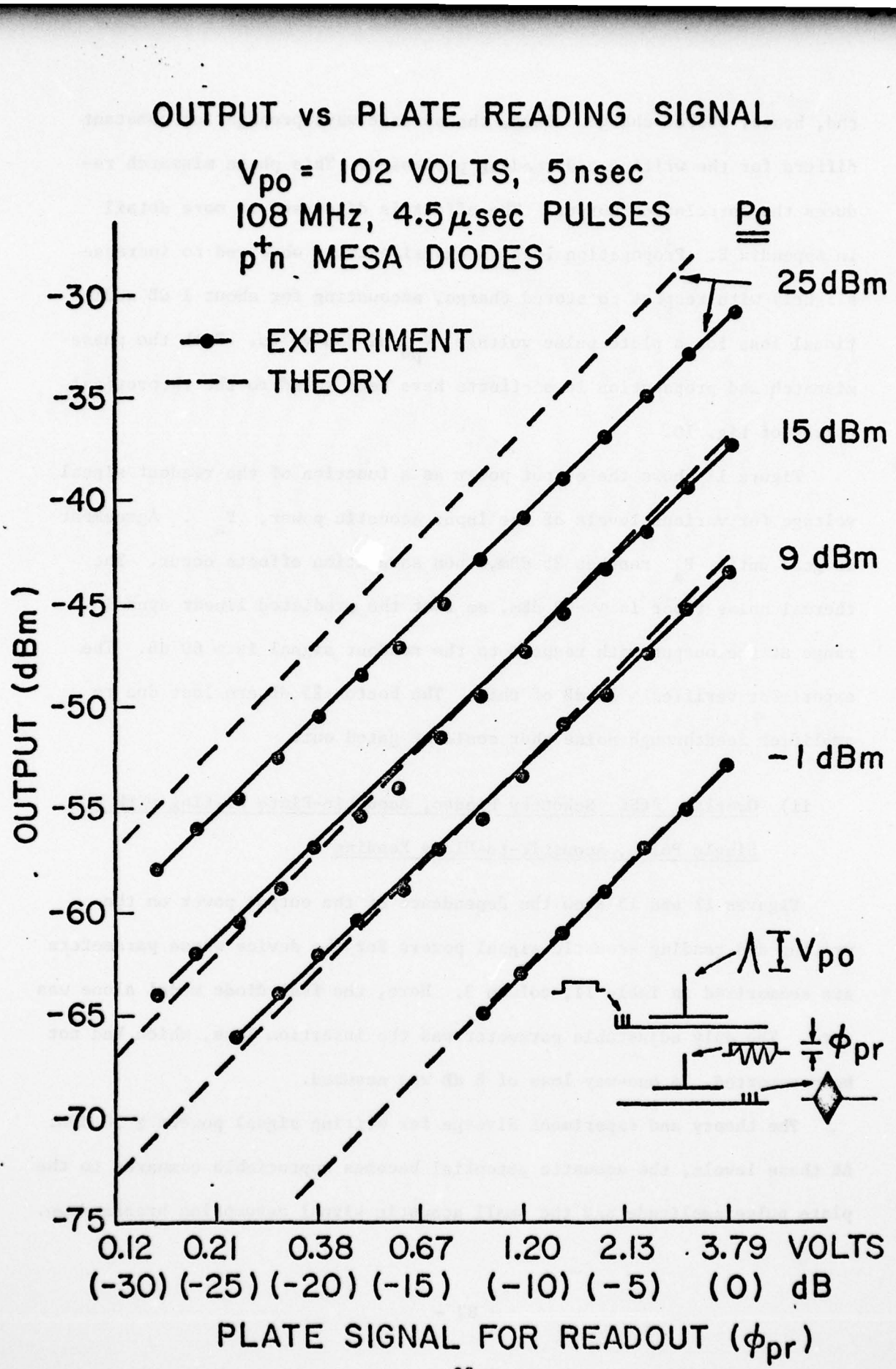
and, hence, stored charge. Thus, the surface wave propagation constant differs for the writing and reading processes. This phase mismatch reduces the correlation output. The effect is discussed in more detail in Appendix B. Propagation loss is experimentally observed to increase slightly with respect to stored charge, accounting for about 1 dB additional loss for a plate pulse voltage V_{p0} of 350 volts. Both the phase mismatch and propagation loss effects have been added to the theoretical curves of Fig. 10.

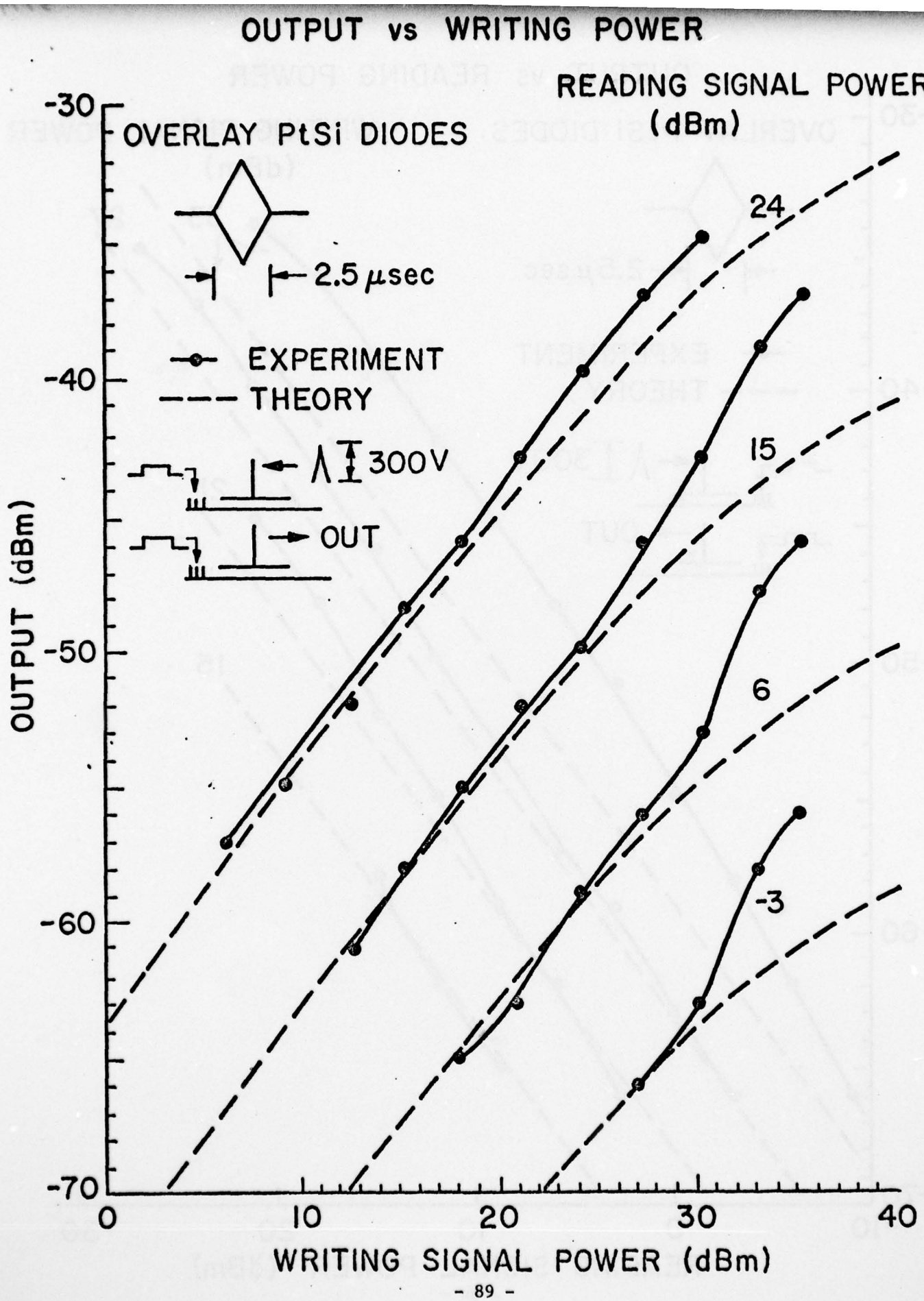
Figure 11 shows the output power as a function of the readout signal voltage for various levels of the input acoustic power, P_a . Agreement is good until P_a reaches 25 dBm, when saturation effects occur. The thermal noise floor is $\sim$ -90 dBm, so that the predicted linear dynamic range at the output with respect to the readout signal is $\sim$ 60 dB. The experiment verifies $\sim$ 35 dB of this. The bottom 25 dB are lost due to amplifier feedthrough noise that could be gated out.

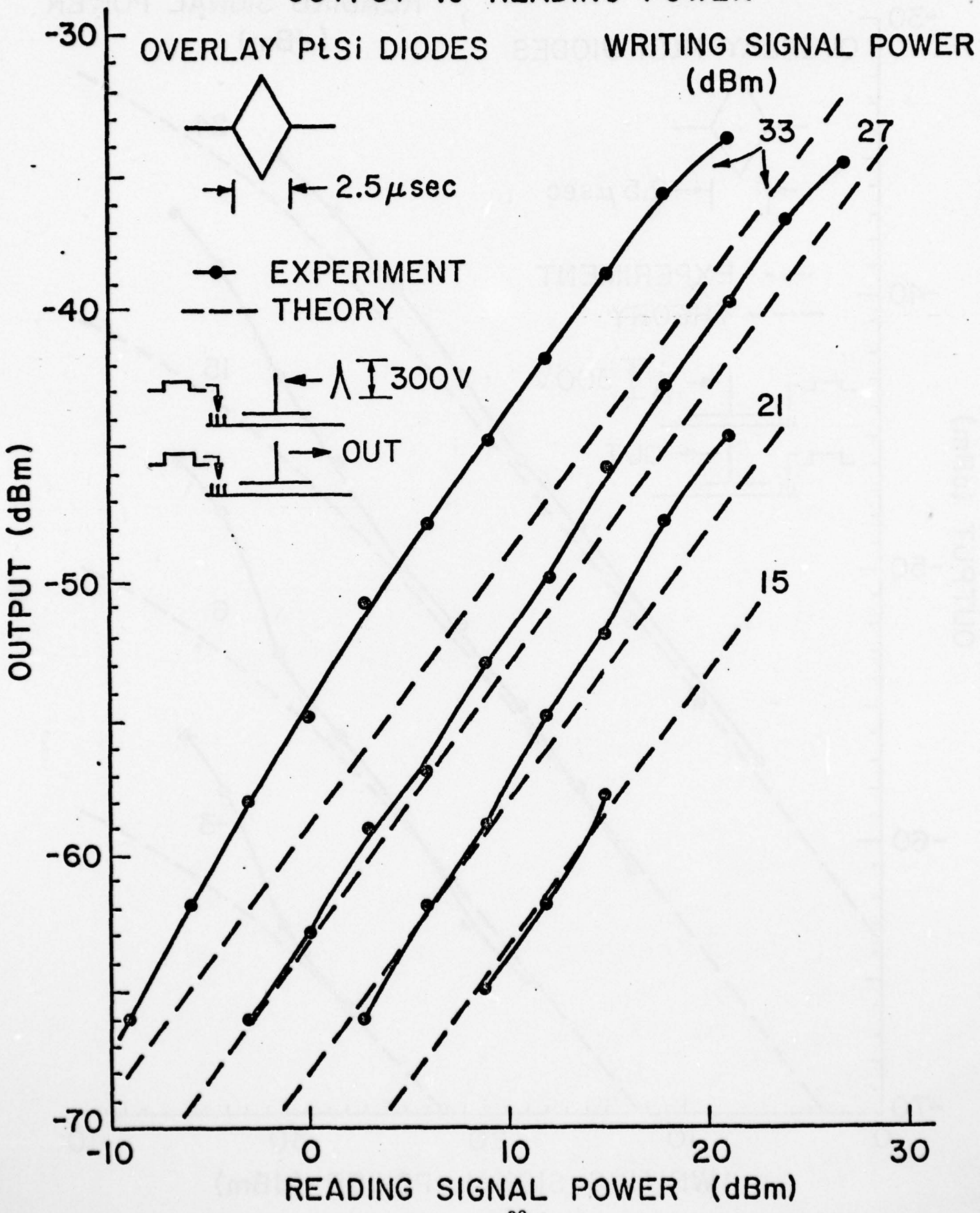
ii) Overlay PtSi Schottky Diodes, Acoustic-Plate Writing with a Single Pulse, Acoustic-to-Plate Reading

Figures 12 and 13 show the dependence of the output power on the writing and reading acoustic signal powers for the device whose parameters are summarized in Table II, column 3. Here, the fast diode model alone was used. The only adjustable parameter was the insertion loss, which had not been reported. A one-way loss of 8 dB was assumed.

The theory and experiment diverge for writing signal powers $\gtrsim$ 30 dBm. At these levels, the acoustic potential becomes appreciable compared to the plate pulse amplitude and the small acoustic signal assumption breaks down.


OUTPUT vs PLATE READING SIGNAL
V_{po} = 102 VOLTS, 5 nsec
108 MHz, 4.5 μsec PULSES
p^+n MESA DIODES
Pa
25 dBm
15 dBm
9 dBm
-1 dBm
EXPERIMENT
THEORY
OUTPUT (dBm)
-30
-35
-40
-45
-50
-55
-60
-65
-70
-75
V_{po}
ϕ_{pr}
0.12 0.21 0.38 0.67 1.20 2.13 3.79 VOLTS
(-30) (-25) (-20) (-15) (-10) (-5) (0) dB
PLATE SIGNAL FOR READOUT (ϕ_{pr})


OUTPUT vs WRITING POWER
READING SIGNAL POWER (dBm)
OVERLAY PtSi DIODES
2.5 μsec
EXPERIMENT
THEORY
300V
OUT
24
15
6
-3
-30
-40
-50
-60
-70
OUTPUT (dBm)
0
10
20
30
40
WRITING SIGNAL POWER (dBm)


OUTPUT vs READING POWER
OVERLAY PtSi DIODES
WRITING SIGNAL POWER
(dBm)
33
27
21
15
2.5μsec
EXPERIMENT
THEORY
300V
OUT
OUTPUT (dBm)
-30
-40
-50
-60
-70
-10
0
10
20
30
READING SIGNAL POWER (dBm)

Such large acoustic potentials may also give rise to interdiode currents. While the result of such effects is not easily predictable, we expect them to cause a breakdown of our theory.

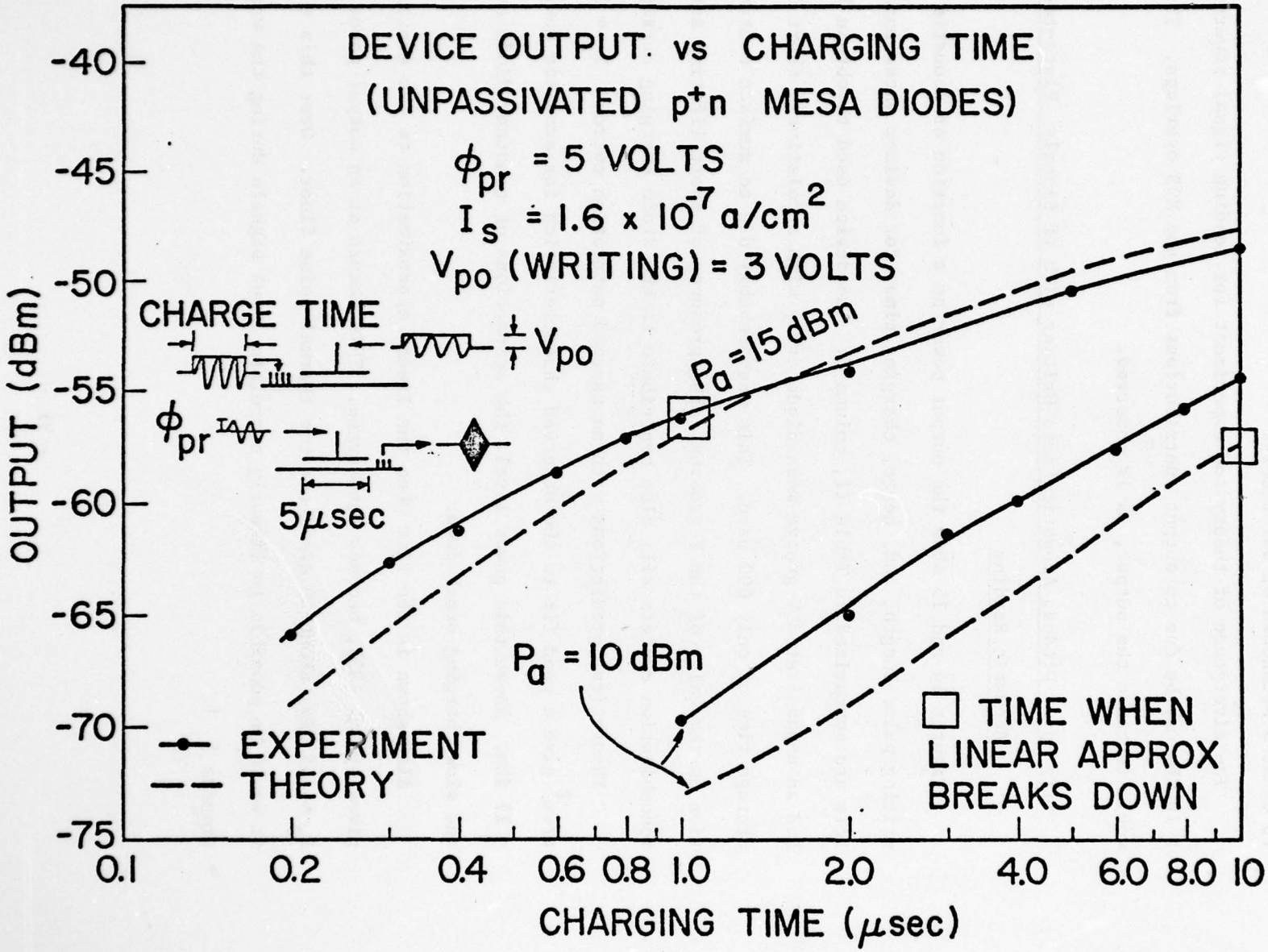
The divergence of theory and experiment for reading signal powers $\gtrsim$ 10 dBm may be due to output contributions from the MOS overlays. This would increase the output, as is observed.

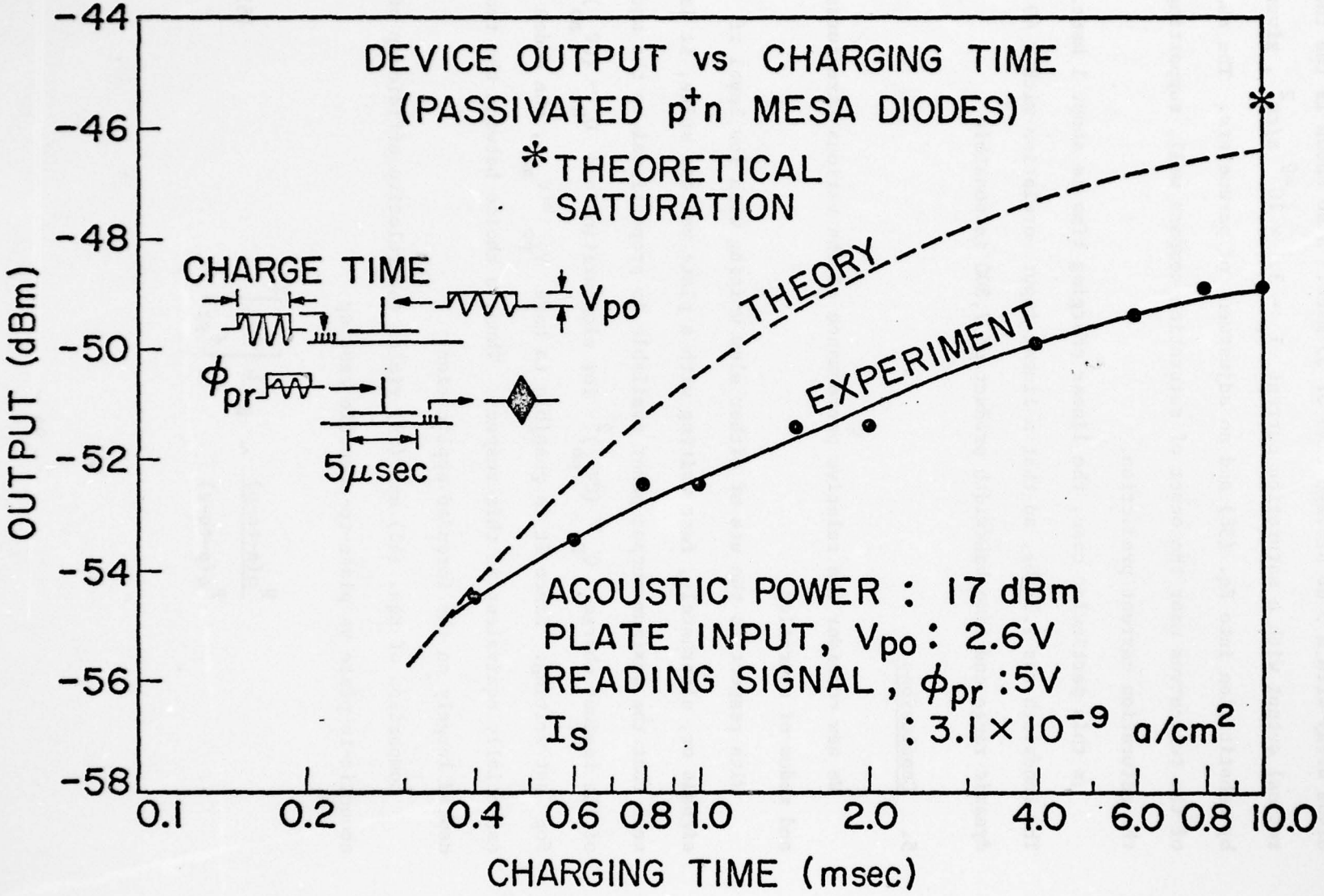
iii) p^+n Diodes, Acoustic-Plate Writing with rf Signals, Plate-to-Acoustic Reading

Figures 14 and 15 show the output power as a function of acoustic writing pulse length, and, hence, charging time, for devices whose parameters are summarized in Table II, column 2. The device used to obtain Fig. 14 had an unpassivated V-groove mesa diode array with a relatively short 3 dB storage time of only 600 μsec. This was probably due to surface contamination on the walls of the V-grooves. The presence of short lifetime surface recombination centers will also contribute to the diode charging currents.

Theoretical predictions with an assumed saturation current $I_s = 1.7 \times 10^{-6}$ a/cm^2 give a good fit to the observed characteristics for acoustic powers $\lesssim$ 17 dBm. Above this power level, the assumptions of constant diode capacity and slow charging break down.

Also shown is the time when the linear approximation to the stored charge, given by Eq. (33), becomes inaccurate. This occurs at an output power $P_0 \sim$ -55 dBm, about 40 dBm above the thermal noise floor. Over this range, it would be possible to linearly correlate input signals during the writing process [ ].


DEVICE OUTPUT vs CHARGING TIME
(UNPASSIVATED p⁺n MESA DIODES)
ϕ_{pr} = 5 VOLTS
I_s = 1.6 x 10^{-7} a/cm²
V_{po} (WRITING) = 3 VOLTS
CHARGE TIME
$\frac{1}{2}V_{po}$
ϕ_{pr}
5μsec
P_a = 15 dBm
P_a = 10 dBm
EXPERIMENT
THEORY
TIME WHEN LINEAR APPROX BREAKS DOWN
OUTPUT (dBm)
-40
-45
-50
-55
-60
-65
-70
-75
0.1
0.2
0.4
0.6
0.8
1.0
2.0
4.0
6.0
8.0
10
CHARGING TIME (μsec)


DEVICE OUTPUT vs CHARGING TIME
(PASSIVATED p+n MESA DIODES)
*THEORETICAL SATURATION
CHARGE TIME
Vpo
φpr
5μsec
THEORY
EXPERIMENT
ACOUSTIC POWER : 17 dBm
PLATE INPUT, Vpo : 2.6V
READING SIGNAL, φpr : 5V
Is : 3.1 × 10-9 a/cm2
OUTPUT (dBm)
-44
-46
-48
-50
-52
-54
-56
-58
0.1
0.2
0.4
0.6
0.8
1.0
2.0
4.0
6.0
0.8
10.0
CHARGING TIME (msec)

The device used to obtain Fig. 15 had a SiO_2 passivated V-groove mesa diode array with a 3 dB storage time of 35 msec. Also shown is the theoretical output with a saturation current $I_s = 3.1 \times 10^{-9}$ a/cm^2, given by substitution into Eq. (38) and no adjustment of parameters. The shapes of the two curves near the onset of saturation compare well, supporting the saturation current prediction.

In this particular case, the linear charging time is about 1 msec. The bandwidth was 7.3 MHz, so that a linear input corelation with a 40 dB dynamic range and time-bandwidth product of 7,300 is possible.

5. Conclusions

We now consider the relative performance of the various structures and modes of operation.

With respect to the use of either slow writing with low level rf signals or, alternately, fast writing with a plate voltage spike, it is seen that the maximum output power available is proportional to the square of the readout charge, $Q_D \approx (CV_{po})^2$ for slow writing and $Q_R \approx (CV_{ao})^2$ for fast writing. Since it is possible to have $V_{po} \approx V_{ao}$, the modes are essentially equivalent in this respect. Thus, a choice between the two would depend largely on the intended application.

Comparison of Eqs. (45) and (59) yields the relative efficiency of acoustic-to-plate vs plate-to-acoustic reading

$$\frac{P_{o(a\text{-}to\text{-}p)}}{P_{o(p\text{-}to\text{-}a)}} \sim 8 \frac{R_L}{Z_a} \left[\frac{\phi_{ar}}{\phi_{pr}}\right]^2 \qquad (65)$$

Comparison of Eqs. (63) and (64) yields the same result for overlay diodes.

Typically, the $Z_a > R_L$. Because of the onset of nonlinear responses both in the piezoelectric substrate and the semiconductor, the maximum acoustic reading signal amplitude ϕ_{ar} is typically an order of magnitude lower than the maximum plate reading signal amplitude ϕ_{pr} . Furthermore, the plate electrode presents a capacitive load. It is thus possible to obtain a large plate reading signal amplitude with external matching while retaining a bandwidth comparable to the transducer limited bandwidth of an acoustic reading signal. For these reasons, plate-to-acoustic reading is more efficient, although, once again, specific design constraints may dictate the choice of reading mode.

Overlays increase the storage time by decreasing the leakage current per unit area. They also enhance efficiency by increasing the effective diode array area. However, a considerable reduction in reading efficiency arises because the readout charge stored in the static overlay capacity cannot contribute to readout. In practice, low leakage, high density p-n diode arrays can offer long storage times and good coverage of the array area without the need of large area overlays. Surface leakage and isolation problems may be averted either through the use of a mesa structure or small area junction shielding overlays.

The performance of p-n junction and Schottky diodes is seen to be essentially equivalent for writing with a plate voltage spike. The significantly lower reverse leakage current allows a p-n diode array to store

a signal for a far longer time. Thus, p-n diodes offer a larger ratio of storage to writing time. We have experimentally demonstrated and reported this elsewhere [15].

With low level signals, p^+n diodes can be charged over longer periods due to their lower saturation current I_s. This is of value in performing correlations during the writing process [16],[17].

Finally, we compare the storage correlator to the acoustoelectric convolver [ ]. The convolver is essentially a storage correlator without storage. Both devices have the same structure; the convolver provides a real time convolution of two opposite traveling acoustic surface waves. It has been conjectured that the two devices have equivalent efficiencies. This may be confirmed by defining an efficiency $\mathcal{M}_{sc}$ for reading mode (a):

$$\mathcal{M}_{sc} = \frac{wV_L}{\sqrt{2P_{aw}P_{ar}}} = \frac{wZ_a}{\sqrt{2}}\left(\frac{C_a}{C_a + C_D}\right)^2 \frac{\text{sinc}^2(\beta\delta/2)}{(V_B - V_D)} \qquad (66)$$

where a value of the load resistor R_L is assumed that gives the peak output power, $R_L = (\omega NLC_p w\delta)^{-1}$, the readout charge is $Q_R = C_a V_a$, the acoustic writing potential $V_a = \sqrt{2Z_a P_{aw}}$, and the acoustic reading potential $\phi_{ar} = \sqrt{2Z_a P_{ar}}$, so that P_{aw} and P_{ar} are the powers of the acoustic writing and reading signals, respectively. An equivalent efficiency for the convolver, $\mathcal{M}_c$, has been shown by Joly [18] to be:

$$\mathcal{M}_c = \frac{wV_0}{\sqrt{2P_{a1}P_{a2}}} = \frac{wZ_a}{2\sqrt{2}} \cdot \frac{(C_a/C_{DO})^2}{[1 + (C_a/C_D)]^3} \cdot \frac{\text{sinc}^2(\beta\delta/2)}{V_B} \qquad (67)$$

where P_{a1} and P_{a2} are the powers of the two opposite propagating acoustic surface waves and V_0 is the device output voltage. Equations (66)

and (67) give:

$$\frac{\mathcal{M}_{sc}}{\mathcal{M}_c} = 2\left[1 + \frac{C_a}{C_D}\right] \quad . \tag{68}$$

Usually, $C_D >> C_a$, and the efficiencies of the two devices are essentially equivalent.

The authors wish to thank John Cafarella of Lincoln Laboratories and Hsing Tuan for their helpful comments and advice, and Robert Joly for his help in characterizing our experimental device.

Appendix A: Diffusion Equation Solutions

In this appendix we solve the p-n junction diode minority carrier diffusion equation to obtain forms for the excess neutral region minority carrier charge in terms of either the diode current or diode voltage.

The diffusion equation is

$$D_p \frac{\partial^2 p_n}{\partial x^2} - \frac{\partial p_n}{\partial t} = \frac{p_n}{T_p} \quad , \tag{A-1}$$

subject to the boundary conditions

$$p_n(0,t) \approx p_{n0} \left(e^{qV_D/kT} - 1\right) \tag{A-2a}$$

$$p_n(x,0) \approx 0 \tag{A-2b}$$

$$p_n(\infty,t) \approx 0 \quad , \tag{A-2c}$$

where $p(x,t)$ is the excess neutral region minority carrier charge, p_{no} is the minority carrier concentration at equilibrium, $V_D(t)$ is the junction voltage, D_p is the minority carrier diffusion constant, and T_p is the minority carrier lifetime.

The use of Laplace transforms allows the direct solution of (A-1), yielding the result

$$p_n(x,t) = \frac{x}{2\sqrt{\pi D_p}} \int_0^t \frac{p_n(0,\tau)\, e^{-\frac{x^2}{4D_p(t-\tau)}}\, e^{-\frac{t-\tau}{T_p}}}{(t-\tau)^{3/2}}\, d\tau \quad . \tag{A-3}$$

The total minority carrier charge Q_p is

$$Q_p = \int_0^\infty p_n(x,t)\,dx = q\sqrt{D_p/\pi}\int_0^t \frac{p_n(0,\tau)e^{-\frac{t-\tau}{T_p}}}{(t-\tau)^{1/2}}\,d\tau \quad . \quad \text{(A-4)}$$

In most cases, these results will be applied for $t << T_p$. Assuming $e^{qV_D/kT} >> 1$, (A-4) becomes

$$Q_p = qp_{n0}\sqrt{D_p/\pi}\int_0^t \frac{e^{qV_D(\tau)/kT}}{(t-\tau)^{1/2}}\,d\tau \quad . \quad \text{(A-5)}$$

Alternately, since the hole current is $I_p(x) = -qD_p(dp/dx)$, Laplace transforms may be used to find a solution to (A-1) of the form

$$p_n(x,t) = \frac{1}{q\sqrt{\pi D_p}}\int_0^t \frac{I_p(0,\tau)\,e^{-x^2/4D_p(t-\tau)}}{(t-\tau)^{1/2}}\,d\tau \quad . \quad \text{(A-6)}$$

Thus, since the total current is $I(0,t) = I_p(0,t)$, Eq. (A-6) takes the form

$$p_n(0,t) = \frac{1}{q\sqrt{\pi D_p}}\int_0^t \frac{I(0,\tau)}{(t-\tau)^{1/2}}\,d\tau \quad . \quad \text{(A-7)}$$

Appendix B: Output Reduction due to Phase Mismatching

It has been assumed that the propagation constant $\beta + \gamma$ under the diode array is constant for both reading and writing. This is not strictly true, since the diode capacitance differs in each operation.

Consider, for example, acoustic-plate writing with a single plate pulse and acoustic-to-plate readout. As the writing surface wave propagates under the diode array, since no charge is stored, the capacity of each array element is the zero bias diode capacity C_{D0} . Due to stored charge, after writing the capacity of each diode array element has changed to C_D , with $C_D \neq C_{D0}$. The surface impedance of the charged and uncharged diode arrays differ; as a result, the propagation constants also differ.

Let us suppose the propagation constant for writing is $\beta + \gamma$ and for reading $\beta + \gamma + \Delta\beta$. The correlation integral over the full array length L takes the form

$$\int_{-L/2f}^{L/2f} e^{-j(\beta+\gamma)z} \, e^{j(\beta+\gamma+\Delta\beta)(z-v_a t)} \, dz \qquad \text{(B-1)}$$

$$\sim \operatorname{sinc} \frac{\Delta\beta L}{2f} \quad ,$$

where v_a is the acoustic propagation velocity and f is a filling factor to account for the diodes covering less than the full diode array length.

We may explicitly calculate the change in propagation constant between writing and reading, $\Delta\beta$, from the Rayleigh wave amplifier theory of Kino and Reeder, Eq. (21),

$$\frac{1}{Y^- - Y_0} = j\left[\frac{M(\beta h)}{\beta\omega\varepsilon_0} - \frac{\beta_a w Z_a(\beta h)}{\beta^2 - \beta_a^2}\right] \qquad \text{(B-2)}$$

with

$$M(\beta h) = \frac{\epsilon_0 + \epsilon_p \tanh \beta h}{(\epsilon_0 + \epsilon_p)(1 + \tanh \beta h)} \quad , \qquad \text{(B-3)}$$

where β and β_a are the perturbed and unperturbed acoustic surface wave propagation constants, respectively, Y^- is the semiconductor admittance, $Y_0 = j\omega\epsilon_0\beta$ is the admittance of free space, and all other quantities have been defined previously.

We set

$$Y^- = j\omega C_D >> Y_0 \quad . \qquad \text{(B-4)}$$

Assuming small perturbations, (B-2) is rearranged to give

$$\frac{(\beta - \beta_a)}{\beta} = \frac{\omega w Z_a}{2\beta\left[\frac{1}{C_a} + \frac{1}{C_D}\right]} \quad , \qquad \text{(B-5)}$$

where we have set $C_a = \epsilon_0\beta/M(\beta h)$, essentially as in Eq. (1). It is noted when $C_a << C_D$, as is usually true, $\beta - \beta_a = \gamma$, in agreement with Eq. (52).

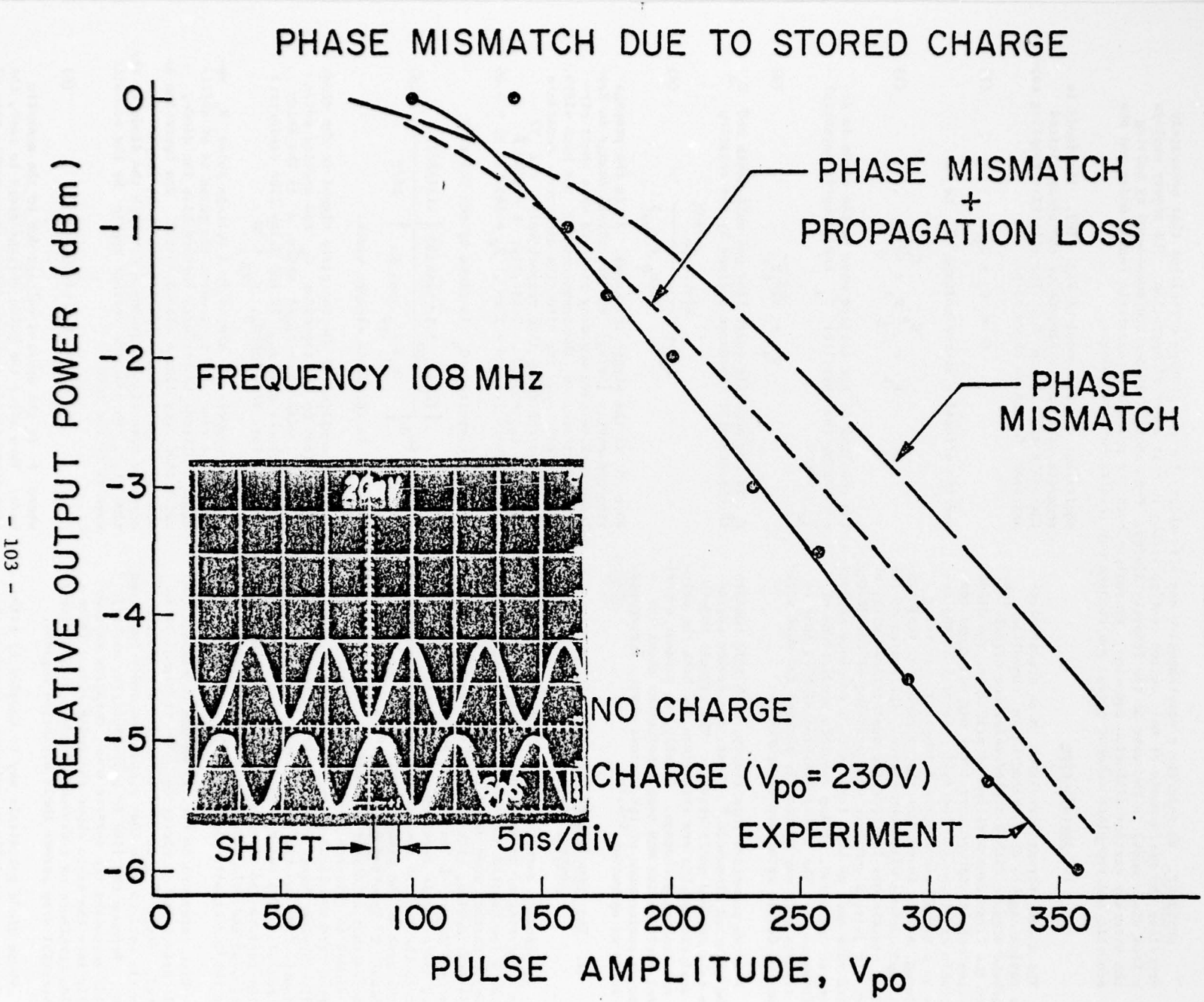
We suppose a diode capacitance of C_{D0} for writing and C_D for reading, with $C_D < C_{D0}$. Then, from Eq. (B-5), the difference in propagation constant between writing and reading, $\Delta\beta$, is given by

$$\Delta\beta = \gamma\left[\frac{1}{1 + (C_a/C_{D0})} - \frac{1}{1 + (C_a/C_D)}\right] \quad . \qquad \text{(B-6)}$$

We have experimentally observed the phase shift due to $\Delta\beta$. The device described in Table II, column 1, was pulsed with a 230 V, 5 nsec plate pulse and the change in propagation delay under the diode array was

measured. Figure 16 shows the observed 3.5 nsec delay of the 108 MHz rf signal that has propagated under the 5 μsec long diode array. This delay is consistent with a filling factor f of 1.26.

The $\text{sinc}^2(\Delta\beta L/2f)$ output power reduction due to phase mismatching is plotted as a function of plate pulse amplitude V_{p0} in Fig. 16. Also shown is the experimentally observed drop in output power with respect to the plate pulse amplitude V_{p0}. This is copied directly from Fig. 10. Adding the experimentally observed increase in propagation loss with respect to V_{p0} accounts for most of the measured drop in output power with respect to the plate pulse amplitude V_{p0}.


PHASE MISMATCH DUE TO STORED CHARGE
RELATIVE OUTPUT POWER (dBm)
0
-1
-2
-3
-4
-5
-6
0
50
100
150
200
250
300
350
PULSE AMPLITUDE, Vpo
PHASE MISMATCH + PROPAGATION LOSS
PHASE MISMATCH
FREQUENCY 108 MHz
NO CHARGE
CHARGE (Vpo= 230V)
EXPERIMENT
SHIFT
5ns/div

APPENDIX B

AN ANALYTIC THEORY FOR THE STORAGE CORRELATOR*

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Edward L. Ginzton Laboratory
Stanford University
Stanford, California 94305

ABSTRACT. We describe a comprehensive analytic theory for the storage correlator that accurately describes the performance of most device configurations in most modes of operation. The theory employs a fast diode model in the case of the Schottky diodes. P-n junction diodes are considered by solving the minority carrier diffusion equation. We analyze both the pulse and parametric readin modes and the acoustic and top-plate readout modes, and compare our results to experiment.

I. Introduction

The diode storage correlator is an acoustoelectric device capable of correlating or convolving[1-4] broadband signals with a stored reference signal. Since the first demonstration of principle, the diode acoustoelectric storage correlator has undergone considerable development. The full potential of the device as a signal processor and imager is now being explored, and it is evident that a number of real systems applications will soon evolve. The design of the storage correlators for specific applications will, of course, require a complete understanding of the device. Toward this end, we have formulated a complete analytic theory of operation, giving accurate predictions of performance.[5,6] The theory features simple, easy to use results that may be readily adapted for most variations of device structure or operation.

Here we summarize this theory, with full results to be reported elsewhere.[6] First, the device operation is described qualitatively. The circuit models and analytic results are then given for both the writing and reading processes. Finally, we present experimental verification and some conclusions about the relative performance of the various device structures and modes of operation.[1-4,7-9]

II. The Principle of Operation of the Storage Correlator

The storage correlator is an acoustoelectric device consisting of an array of semiconductor diodes spaced a few hundred nanometers above a piezoelectric acoustic surface wave delay line (Fig. 1). It is a three-port device, with interdigital acoustic surface wave transducers L and R at each end of the delay line, and a single terminal T consisting of a contact to the back of the diode array and a ground plane on the back of the piezoelectric delay line. This terminal T is often called the "top plate." It will be noted that no direct connection is made to individual diodes in this configuration. A signal may be written into the diode array, in the form of a spatially varying charge pattern, through the interaction of inputs from any two ports. Readout is obtained at the top plate (T) due to the interaction of the stored charge pattern and an acoustic reading signal. Alternately, an acoustic readout may be obtained in response to a reading signal, applied to the top plate.

With reference to Fig. 1, we can understand the basic principles of operation. The rf signal to be stored, $F(t)e^{j\omega t}$, is used to excite a traveling acoustic surface wave that propagates under the diode array. Because the line is peizoelectric, electric fields accompany the surface wave, decaying exponentially into the space above the delay line. These fields terminate on individual diodes, giving rise to a potential drop across their depletion regions.

These diode potentials may be sampled by using the devices essentially as switches. Consider the equivalent circuit model of Fig. 1(c). The diode is regarded as a single element of the array excited through a capacitance C. The effective coupling capacitance C can be shown to be

$$C = C_a + C_p \tag{1}$$

and the effective source voltage V_s to be

$$V_s = \frac{C_a}{C} V_a + \frac{C_p}{C} V_p \quad . \tag{2}$$

The coupling of the surface wave to the diode is described by the capacitor C_a and acoustic potential V_a, where

$$V_a = \sqrt{2P_a Z_a} \tag{3}$$

P_a is the acoustic power flow per unit width and Z_a is the acoustic impedance defined by the relation

$$Z_a = \frac{2|\Delta v/v_a| e^{-2\beta h}}{\omega w(\epsilon_0 + \epsilon_{pa})} \quad . \tag{4}$$

Here h is the airgap thickness, β is the propagation constant, $|\Delta v/v_a|$ the fractional change in Rayleigh surface wave velocity produced by a short circuited surface, ω the frequency, w the beam width, and ϵ_0 and ϵ_{pa} the effective dielectric constants of air and the delay line respectively. For YZ - $LiNbO_3$, $\epsilon_{pa} = 50.2$. Typically, $h = 3000$ Å, $\omega = 100$ MHz $\times 2\pi$, $w = 1$ mm, $Z_a = 140\,\Omega$, $\beta h = 0.06$.

The capacitor C_s is given by the relation

$$C_a = \beta\epsilon_0 \left[\frac{(\epsilon_0 + \epsilon_{pa})(1 + \tanh \beta h)}{\epsilon_0 + \epsilon_{pa} \tanh \beta h} \right] \frac{\sin(\beta\delta/2)}{\beta\delta/2} \tag{5}$$

Here, δ is the diode element width.

The coupling of the top plate signal to the diode is described by the capacitor C_p and applied potential V_p, with $C_p = \epsilon_{yy}/d$ where d is the delay line thickness and ϵ_{yy} is the delay line dielectric constant for YZ - $LiNbO_3$, $\epsilon_{yy} = 70$.

Now suppose the source is a voltage pulse V_p applied at a time $t = t_p$, where the pulse is of sufficient amplitude to strongly forward bias the diode, which then acts like a closed switch. The operation is that of a sample and hold circuit, which samples the acoustic wave signal passing underneath the diode at the time t_p. Suppose the voltage applied by the acoustic wave is of the form

$$V_a = V_{a0} \sin(\omega t - \beta z) \tag{6}$$

where β is the applied voltage due to the acoustic wave. Then after the pulse voltage drops to zero, the capacitors retain a charge due to the acoustic wave of

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the form

$$Q = CV_s = C_p V_{p0} + C_a V_{a0} \sin(\omega t_p - \beta z) = Q_p + Q_R \quad (7)$$

where Q_R is the spacially varying component of Q.

Once the pulse voltage drops to zero, the diode is reverse biased and acts like a varactor.

If we suppose that $C_p << C_D$, the capacitance of the diode, we can write, in general, that $Q \approx Q_D$ where Q_D is the diode charge, given by the relation

$$Q_D = \sqrt{2qN_S\epsilon_s V_B} - \sqrt{2qN_D\epsilon_s(V_B - V_D)} \quad (8)$$

$$= C_{DO}V_B - C_D(V_B - V_D)$$

with

$$C_D = \left[2qN_D\epsilon_s/(V_B - V_D)\right]^{1/2}, \quad (9)$$

where V_B is the built-in voltage of the diode, N_D its doping, ϵ_s its dielectric constant, C_D its large signal capacity and C_{DO} its capacity when $V_D = 0$, with $Q_{DO} = C_{DO}V_B$. Under reverse biased conditions, where V_D is negative, we can write

$$\frac{1}{C_D} = \frac{1}{C_{DO}}\frac{Q_{DO} - Q_D}{Q_{DO}} \quad (10)$$

so the spatially varying component of $1/C_D$ is $Q_R/Q_{DO}C_{DO}$. On readout we apply a voltage $\Phi_{PR}\sin\omega t$ to the plate as shown in Fig. 3. This in turn develops a voltage across the diode capacitance of value

$$V_D \approx \frac{C_p\Phi_{PR}\sin\omega t}{C_D} \quad (11)$$

So from Eqs. (10) and (11) the spatially V varying voltage component developed at the diodes is of the form

$$V_{DR} = \frac{C_p C_a V_{a0}\Phi_{PR}\sin(\omega t_p - \beta z)\sin\omega t}{C_{DO}V_B}. \quad (12)$$

We note that this voltage is independent of the original pulse voltage applied, but is linearly proportional to the acoustic signal read into the device as well as the readout signal Φ_R. It has the same frequency variation as the input signal and two components of spatial variation $\pm\beta z$. These correspond to both forward and backward propagating acoustic surface waves.

Thus the principle of operation on reading is to use the diodes as sample and hold circuits which retain charge. On readout the spatial variation of the capacitances of the diodes due to the retained charge is such that a readout voltage applied to the plate excites the diodes with the same spatial variation. This in turn excites forward and backward propagating waves, whose amplitudes can be determined by normal mode theory.

III. Detailed Analysis of the Writing Process

A more complete analysis of the reading processes has been carried out for the following situations:

(a) Fast charging. This is the case described in the previous section. A single sampling pulse is used to fully charge the device.[1,2,3]

(b) Slow charging. Here, the sampling pulse is of insufficient amplitude to strongly forward bias the diodes, and a single pulse allows only a small amount of charge to be stored. By employing a long train of pulses, however, the device may be fully charged.[3,5,7]

The device structures considered are:

(a) Fast diodes. A fast diode such as a Schottky diode is a device that responds to all applies signals with an I-V characteristic of the form

$$I = I_s(e^{qV_D/nkT} - 1),$$

independent of frequency at least in the range of interest. Here, I_s is the saturation current and V_D is the diode voltage.[1,2]

(b) p^+n - junction diodes. p^+n diodes do not, in general, behave like fast diodes at the typical frequencies of operation used. We have solved the p^+n junction diffusion equation to account for their transient characteristics. We find that, with sufficient applied voltage p^+n diodes can be charged rapidly because minority carrier charge moves across the depletion layer essentially instantaneously.[3,4,5,7-10]

(c) Overlay structures. The theory is readily adapted to overlay Schottky or p-n diodes. For the case of a constant overlay capacitance, analytic results are obtained.[1-4]

(a) Fast diodes. To find the stored charge, we write the current equation for the circuit model (2a) as

$$C\frac{d}{dt}(V_S - V_D) = \frac{dQ_D}{dt} + I_s e^{qV_D/kT} \quad (13)$$

Here, the diode current is due to both conduction current, the second term on the right hand side of Eq. (13); and displacement current through the depletion layer, the first term on the right hand side of of Eq. (13). Q_D is the diode charge where now we take account of the diode capacity by using Eqs. (8) and (9).

We note that when V_D is small, so no conduction current flows, the solution of Eq. (13) is $Q_D = C(V_S - V_D) + \text{constant}$. But when current flows momentarily as V_D reaches its peak value, the value of Q_D changes. It is therefore convenient to define a parameter $Q_S(t)$ as follows:

$$Q_S(t) = Q_D - C(V_s - V_D). \quad (14)$$

The charge in Q_D due to the "pip" of current when V_D reaches its peak value is $-Q_S$. Hence we call Q_S the stored charge.

Equation (13) can now be written in the form

$$\frac{dQ_S}{dt} = I_S e^{qV_D/kT}. \quad (15)$$

This has the solution for the stored charge $Q_S = \text{constant}$ when the conduction current is small, as would be expected, and can be solved fairly easily for other cases, by substitution of Eq. (14) in the right hand side of Eq. (15) provided it is assumed that $C_D = C_{Dp} = \text{constant}$ when the diode voltage is near its peak at time $t = t_p$.

We have considered individual cases of fast and slow charging. The pulse on the plate is assumed

parabolic in shape, so that the source voltage is of the form

$$V_S(t) = \frac{C_a}{C} V_{a0} \sin(\omega t - \beta z) + \frac{C_p}{C} V_{p0} \left[1 - \left(\frac{t-t_p}{t_p}\right)^2\right] . \quad (16)$$

It can be shown by solving Eq. (15) that the required solution is

$$V_D(t) = \frac{C}{C_T}\left[V_S - V_S(t_p)\right] + \frac{V_B}{C_T}(C_D - C_{Dp}) - \frac{kT}{q}\frac{C_{Tp}}{C_T} \times \ln\left[I_s\sqrt{\frac{\pi q}{kTC_T C_p V_{p0}}}\right] \quad (17)$$

where $C_T = C_D + C$, $C_{Tp} = C_{Dp} + C$.

The positive top plate voltage required to strongly forward bias, or "turn-on" the diode, V_{on} , is defined to be reached when the coupling capacitor charge $C(V_s - V_{Dp})$ and stored charge Q_S at the saturation voltage V_{Dp} are equal. Thus,

$$V_{on} = \frac{C_a V_{a0}}{C_T} + \frac{V_B}{C_p}(C_{D0} - C_{Dp}) - \frac{kT}{q}\frac{C_{Tp}}{C_p} \times \ln\left[I_s t_p\sqrt{\frac{\pi q}{kTC_{Tp} C_p V_{p0}}}\right] \quad (18)$$

We find also that the spatially varying component of Q that is stored by diodes is precisely the last term of Eq. (7) as would be expected.

(b) Slow charging, with a pulse train. We assume a source voltage of the form

$$V_S = \frac{C_a V_{a0}}{C}\sin(\omega t - \beta z) + \frac{C_p V_{p0}}{C}\sin\omega t . \quad (19)$$

We assume $e^{qV_{a0}/kT} >> e^{qV_{p0}/kT}$, and V_{a0} of sufficiently low amplitude so that the diode displacement current dominates. In this case it can be shown that for large times the spatially varying component of readout charge has the symptotic form

$$Q_R = C_p V_{p0} \cos\beta z . \quad (20)$$

For short times, the readout charge varies linearly with time, and has the form

$$Q_R = 2I_s t I_0\left(\frac{q}{kT} V_{a0}\frac{C}{C_T}\right) I_1\left(\frac{q}{kT} V_{p0}\frac{C}{C_T}\right)\cos\beta z \quad (21)$$

where I_0 and I_1 are modified Bessel functions. We note that for V_{p0} sufficiently small $Q_R \propto V_{p0}$, i.e., it varies linearly.

(c) p^+n Diodes

1. Fast charging with a single pulse. We have shown, by solving the p^+n junction diffusion equation for times much shorter than the minority carrier lifetime, that the excess minority carrier density at the edge of the neutral region, $p_n(0,t)$, is

$$p_n(0,t) = p_{n0}\left(e^{qV_D/kT} - 1\right) = \frac{1}{q\sqrt{\pi D_p}}\int_0^t \frac{I_D \tau}{(t-\tau)^{1/2}} d\tau \quad (22)$$

where D_p is the hole diffusion constant, p_{n0} the equilibrium hole density, and $I_D(t)$ the diode current. We again assume a parabolic top plate pulse, so that the source voltage is given by Eq. (16). Since the voltage drop is largely across the coupling capacitor C , the diode current is linear and, from Eqs. (22) and (16), the diode voltage during charging is given by the relation

$$V_D(t) = \frac{kT}{q}\ln\left[1 + \frac{4CV_{p0}}{qp_{n0}t_p}\sqrt{t/\pi D_p}\left(1 - \frac{2}{3}\frac{t}{t_p}\right)\right] \quad (23)$$

We see that the diode voltage rapidly saturates, remaining constant until $t = 3t_p/2$, when it rapidly drops to zero. At this time, the source voltage V_s has dropped to 3/4 of its peak value. For $t > 3t_p/2$, $V_D < 0$, and all diode current ceases to flow. Thus, the diode acts like a fast diode in this application but returns only 75% of the charge that a fast diode would retain.

2. Slow charging with p^+n diodes. It is also possible to express the total excess minority carrier charge in the neutral region in terms of the diode voltage V_D . Assuming that the conduction current is small compared to the displacement current through the diodes, by use of Eq. (8) we can find the stored charge for slow charging of p^+n diodes. The results are identical to those for the fast diode Eqs. (20) and (21) with a saturation current I_S given by the relation

$$I_S = \frac{qp_{n0}}{\pi}\sqrt{\frac{2\omega D_p}{3}} \quad (24)$$

For a typical value of $N_D = 4.6 \times 10^{14}/cm^3$, $p_{n0} = 5.6 \times 10^5/cm^3$, with $\omega = 6.28 \times 10^8\ sec^{-1}$, $D_p = 20\ cm^2/sec$, we find $I_S = 2.6 \times 10^{-9}\ a/cm^2$. This is about 100 times less than the value of I_S for a PtSi Schottky diode.

(c) Overlays. An overlay may be modeled as a capacitance in parallel with the diode depletion layer. This does not change the qualitative form of the above results, since the overlay can only increase the diode capacity.

(d) Writing with two acoustic inputs. Usually the diode potentials due to the acoustic surface waves are weak, so that the diode displacement current dominates. The analysis is identical in form to that for slow charging, with one of the acoustic signals and coupling capacity C_a replacing the top plate signal and coupling capacitor C_p .[3,9]

IV. ANALYSIS OF THE READING PROCESS

We have found the device output power in terms of the stored readout charge Q_R , found in the previous section, and the reading signal amplitude. Results have been for both plate-to-acoustic reading, where an acoustic output appears in response to a plate reading signal, and acoustic-to-plate reading, where a plate output appears in response to an acoustic reading signal. We describe here only the plate-to-acoustic reading results.

We follow the analysis given in Section II to find the voltage developed across the diodes in the form of Eq. (12).

The amplitude of the surface wave excited by this component of diode potential is found using the normal mode theory of Kino and Auld.[12,13] By direct substitutions into Eq. (31) of this reference, and solving for

the potential due to the fundamental acoustic mode ϕ_a, in terms of the total rf potential[13] the output power is found to be

$$P_0 = \frac{1}{2Z_a}\left[\frac{\gamma L\delta}{\ell}\right]^2\left[\frac{C_p \phi_{PR} Q_R}{2C_{DO}^2 V_B}\,\mathrm{sinc}\,\frac{\beta\delta}{z}\right]^2 \qquad (25)$$

where L is the interaction region lengths, ℓ the diode array period, and γ the perturbation of the acoustic propagation constant β due to the presence of the diode array. γ is a measure of the coupling of the diode potential back to the acoustic surface wave, and is given by the relation

$$\gamma = \frac{\omega w C_a Z_a}{2} \quad . \qquad (26)$$

A very similar analysis has been carried out for acoustic-to-plate readout. This is given elsewhere.[6]

V. Comparison to Experiment

Here we present sets of experimental results that verify most aspects of the above theory. The data has been obtained with a number of different devices. Their parameters are summarized in Table 1.

P^+N Junction Diodes

Single pulse writing, plate-to-acoustic reading. The output power is shown as a function of plate pulse height in Fig. 4 for the device whose parameters are summarized in Table 1, column 1. The theoretical output is plotted with no adjustment of parameters, beginning at the turn-on voltage V_{On}. The fast diode model was used in conjunction with the -2.5 dB correction for p^+n diodes, as follows from p-n diode theory (75% of the charge retained). The theory is seen to accurately predict both the turn-on voltage, V_{On}, and output power.

We have observed V_{On} to be independent of temperature.[5] This is consistent with the predicted diode voltage, given in Eq. (23), since $1/p_{n0} \sim n_i^2 \sim \exp(E_g/kT)$ where n_i is the intrinsic carrier concentration and E_g the bandgap energy.

These results indicate that p^+n diodes perform very much like fast diodes. With pulses of sufficient amplitude, they can be completely charged in times on the order of a few nanoseconds. This process utilizes minority carrier drift across the depletion region, rather than generation or recombination, and is independent of the storage time. By employing p^+n diodes, it is thus possible to demonstrate a device that charges in nanoseconds and stores for seconds. We have, in fact, shown this at low temperatures.[5]

The drop in output for increasing plate pulse height is largely due to a phase mismatch between the writing and reading process due to the charge in diode capacity.

Propagation loss is observed to increase slightly with respect to charging pulse height, accounting for about 1 dB additional loss for a plate pulse voltage of 350 V. Both this and the phase mismatch effects have been added to the theoretical curves of Fig. 4.

The output power vs reading signal voltage is plotted in Fig. 5 for various levels of input acoustic power, P_a. Agreement is good for an acoustic input power $P_a \lesssim 25$ dBm, with a thermal noise floor of -90 dBm, the predicted linear dynamic range of the output with respect to the reading signal is ~ 60 dB. The experiment verifies ~ 35 dB of this, the lower 25 dB part is due to amplifier noise that could be gated out.

Slow writing with rf signals, plate-to-acoustic reading. Figure 6 shows the device output power as a function of time for the device whose parameters are summarized in Table 1, column 2. The theoretical curve is again plotted with no adjustment of parameters, using a calculated saturation current of $I_S = 3.1 \times 10^{-9}$ a/cm^2. The accuracy here is a critical function of the device parameters, since the output and time for the onset of saturation are both essentially exponential functions of the applied voltages and the inverse of the diode capacitance C_D.

For this particular case, the linear charging time is about 1 msec. The bandwidth was 7.3 MHz, so that a linear correlation of input signals[7,8,9] with 40 dB dynamic range and time-bandwidth product of 7300 is possible.

Schottky Diodes with Overlays, Single-Pulse Writing, Acoustic-to-Plate Reading

Figure 7 shows the dependence of the output power on the writing acoustic signal power for the device whose parameters are summarized in Table 1, column 3. These results were obtained and reported by Ingebrigtsen.[2] The fast diode model modified to take account of a fixed diode overlay capacity was used to obtain the theoretical curves. The only adjustable parameter was the insertion loss, which was not reported. A one-way loss of 8 dB for the correlation mode of operation was assumed.[11]

The theory and experiment diverge for writing signal powers $\gtrsim$ 30 dBm. At these levels, the acoustic and plate potentials seen at the diode become comparable, and the small acoustic signal assumption breaks down. Such large acoustic potentials may also give rise to interdiode currents. While the result of such effects is not easily predicted, we expect them to result in breakdown of the theory.

VI. Conclusions

We now consider the relative performance of some of the various structures and modes of operation.

With respect to the use of either slow writing with low level rf signals or, alternately, fast writing with a plate voltage spike, it is seen that the maximum output power available is proportional to the square of the readout charge, $Q_R \approx (CV_{p0})^2$ for slow writing and $Q_R \approx (CV_{a0})^2$ for fast writing. Since it is possible to have $V_{p0} \approx V_{a0}$, the modes are essentially equivalent in this respect. Thus, a choice between the two would depend largely on the intended application.

The performance of p-n junction and Schottky diodes is seen to be essentially equivalent for writing with a plate voltage spike. The significantly lower leakage current allows a p-n diode array to store a signal for a far longer time. Thus, p-n diodes offer a larger ratio of storage-to-writing time. We have experimentally demonstrated and reported this elsewhere.[6]

With low level signals, p^+n diodes can be charged over longer periods due to their lower saturation current I_S. This is of value in performing correlations during the writing process.[8,9,10]

Finally, we compare the storage correlator to the acoustoelectric convolver. The convolver is essentially a storage correlator without storage. Both devices have the same structure; the convolver provides a real time

TABLE 1

Experimental Device Parameters

	(1)	(2)	(3)[2,11]
Writing:	Acoustic-plate (pulse)	Acoustic-plate (rf)	Acoustic-plate (pulse)
Reading:	Plate-to-acoustic	Plate-to-acoustic	Acoustic-to-plate
Plate pulse duration ($2t_p$)	5 nsec	--	5 nsec
One way loss	8.5 dB	10.5 dB	8 dB(assumed)
3 dB storage time	8 msec		∿ 20 msec
Diodes	V-groove isolate mesa p^+n	35 msec	overlay PtSi Schottky
Substrate doping	11 Ω-cm		34 Ω-cm
Overlay contacts	---		10 × 10 μm Cr/Au
Diode diameter	---		5 μm
Diode width (δ)	4 μm		--
Diode period (ℓ)	8 μm		12.5 μm
Interaction length (L)	1.57 cm		0.44 cm
$LiNbO_3$ thickness (d)	450 μm		710 μm
Airgap height (h)	300 nm		200 nm
Airgap spacer	rails		posts
Beam width (w)	1 mm		2.75 mm
Center frequency	108 MHz		65 MHz

convolution of two opposite traveling acoustic surface waves. It has been conjectured that the two devices have equivalent efficiencies. This may be confirmed by defining an efficiency $\mathcal{M}_{sc}$ for acoustic-to-plate reading:

$$\mathcal{M}_{sc} = \frac{wV_L}{\sqrt{2P_{aw}P_{ar}}} = \frac{wZ_a}{\sqrt{2}}\left(\frac{C_a}{C_a+C_D}\right)^2 \frac{\mathrm{sinc}^2(\beta\delta/2)}{(V_B - V_D)} \qquad (27)$$

where a value of the load resistor R_L is assumed that gives the peak output power $R_L = (\omega N L C_D w\delta)^{-1}$, the readout charge is $Q_R = C_a V_a$, the acoustic writing potential $V_a = \sqrt{2Z_a P_{aw}}$, and the acoustic reading potential $\varphi_{ar} = \sqrt{2Z_a P_{ar}}$, so that P_{aw} and P_{ar} are the powers of the acoustic writing and reading signals, respectively. An equivalent efficiency for the convolver, $\mathcal{M}_c$, has been shown by Joly[10] to be:

$$\mathcal{M}_c = \frac{wV_0}{\sqrt{2P_{a1}P_{a2}}} = \frac{wZ_a}{2\sqrt{2}} \cdot \frac{(C_a/C_{D0})^2}{[1+(C_a/C_D)]^3} \cdot \frac{\mathrm{sinc}^2(\beta\delta/2)}{V_B} \qquad (28)$$

where P_{a1} and P_{a2} are the powers of the two opposite propagating acoustic surface waves and V_0 is the device output voltage. Equations (27) and (28) give

$$\frac{\mathcal{M}_{sc}}{\mathcal{M}_c} = 2\left[1 + \frac{C_a}{C_D}\right] . \qquad (29)$$

Usually, $C_D >> C_a$ so the efficiency of the correlator is essentially 6 dB better than that of the convolver.

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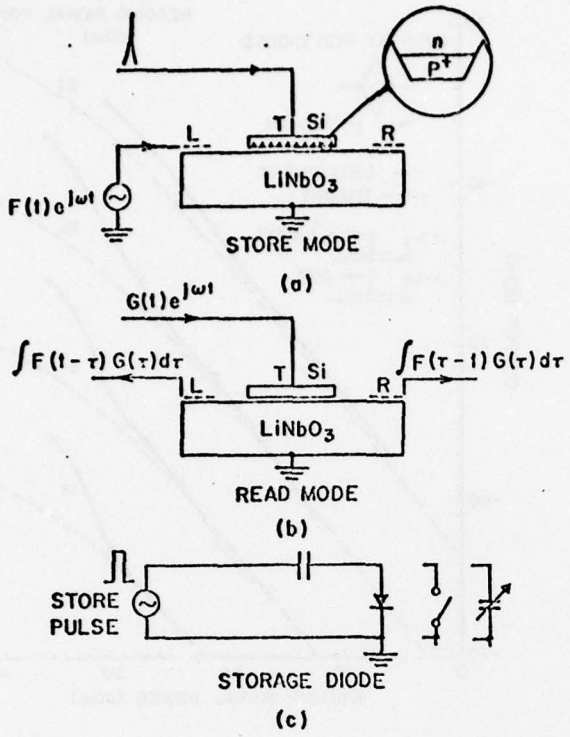

FIG. 1--Storage correlator operation (a) writing process; (b) reading process, and (c) simplified equivalent circuit.

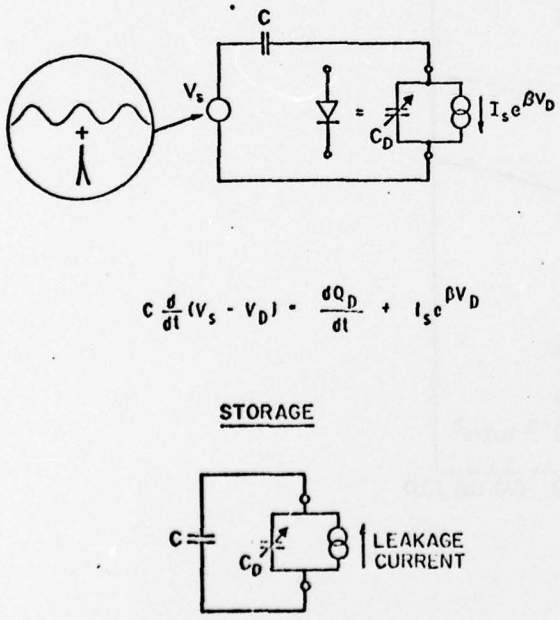

FIG. 2--Equivalent circuits for (a) charging process and (b) storage process.

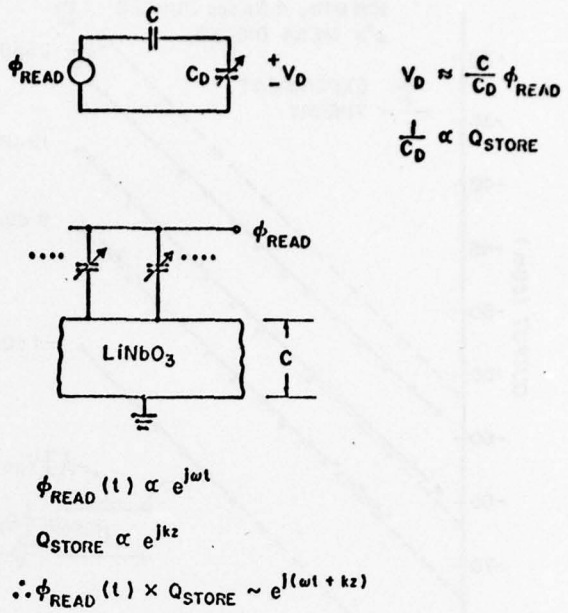

FIG. 3--Equivalent circuit model for plate-to-acoustic reading.

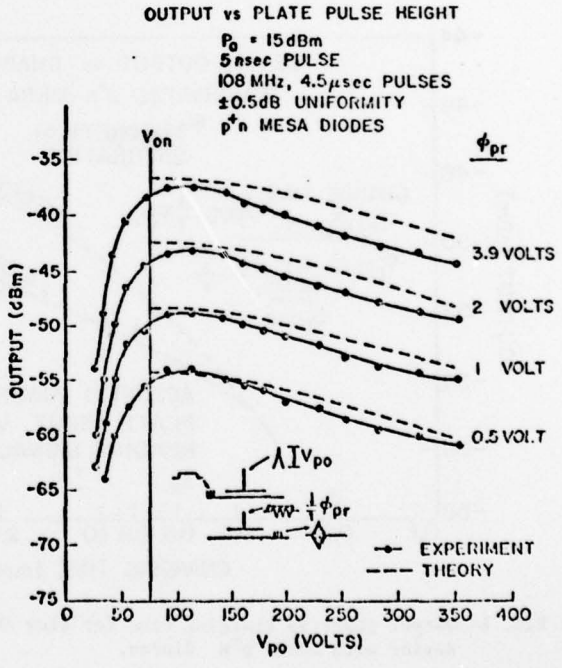

FIG. 4--Output power vs plate pulse amplitude for device with meas p^+n diodes.

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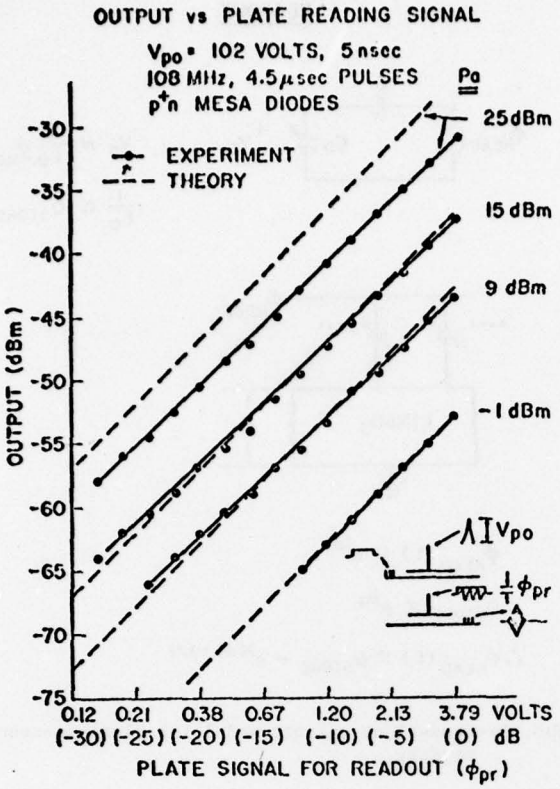

FIG. 5--Output power vs plate reading signal amplitude for device with p^+n diodes.

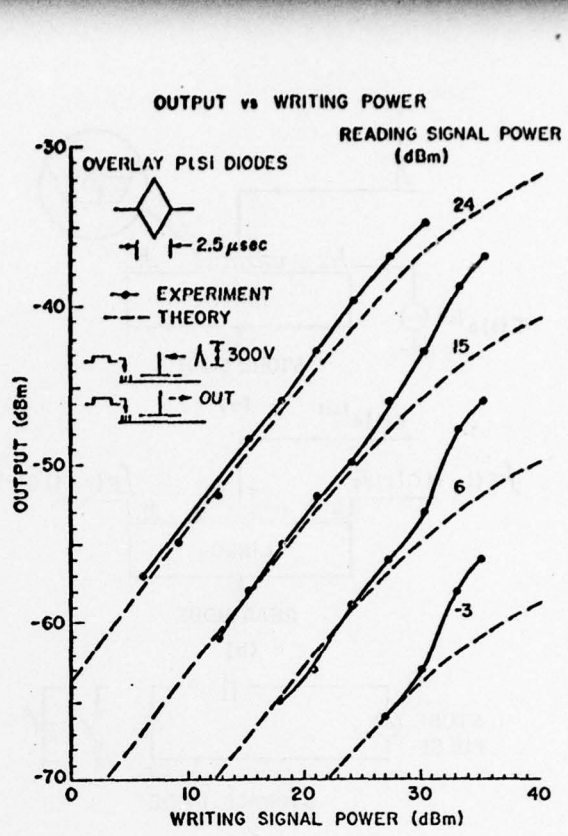

FIG. 7--Output power vs writing signal power for device with overlay Schottky diodes. Experimental data due to Ingebrigtsen.[2]

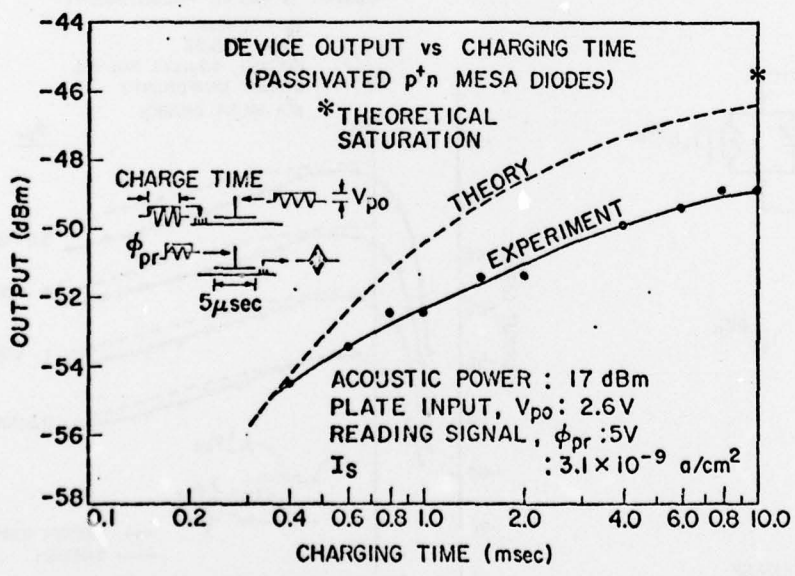

FIG. 6--Output power vs charging time for slow charging device with mesa p^+n diodes.

APPENDIX C

A NEW ZINC-OXIDE-ON-SILICON MONOLITHIC STORAGE CORRELATOR*

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ABSTRACT: A new zinc-oxide-on-silicon monolithic storage correlator using a p-n diode array has been successfully fabricated. Preliminary studies show that the spurious bulk wave generation which severely limits the dynamic range of the air-gap device is absent from this monolithic structure. Therefore, larger dynamic range (>50 dB) is expected. A number of signal processing functions have been demonstrated using this monolithic device with electronic efficiency comparable to that obtained with the air-gap devices. In one experiment, correlation of signals with a time-bandwidth product of 30,000 has been obtained.

I. Introduction

The ASW storage correlator has been investigated intensively in the past three years.[1,2,3] Up until now, almost all of them are of the so-called air-gap type. This air-gap structure has the advantage of being very flexible so that storage correlators made from different combinations of piezoelectric and semiconducting materials can be investigated relatively easily. It also offers a convenient way of studying the performance of different kinds of diode arrays. But, on the other hand, it requires sophisticated assembly techniques, and suffers from excessive spurious bulk wave generation at readout. It is very difficult, if not impossible, to eliminate this spurious bulk wave generation, and the input dynamic range of the device is thus limited to 25 - 35 dB at the present time.

In this paper, we describe a monolithic zinc-oxide-on-silicon p-n diode storage correlator. We begin with a description of the structure and the fabrication technology of our storage correlator. In the second section, the performance and some unique features of this monolithic device will be discussed. The last section is devoted to demonstrating some of the powerful signal processing capabilities of this device by using the so-called input correlation technique.

II. Fabrication of the Monolithic Storage Correlator

Figure 1 is a schematic diagram of the zinc-oxide-on-silicon p-n diode storage correlator. The starting material is 10 - 15 Ω-cm n-type (111) silicon cut along the $(11\bar{2})$ direction. A p-n diode array is laid down in the material; this array has an overall periodicity of 8 μm with each individual diode 4 μm wide. The processing requires one shallow boron diffusion (≈ 0.6 μm) into the n-type substrate, following a n^+ gettering phosphorus diffusion on the back side. This gettering process reduces the number of metallic ions present at the silicon surface, thus improving the reverse bias characteristic of the diodes. At both ends of the substrate, a gold layer 2000 Å thick is evaporated at 230°C onto a thin layer of titanium produced by a flash evaporation. The (111) oriented gold layers form excellent underlayers for the later ZnO growth; they provide large shorting planes underneath the interdigital transducers so that the transducers can be excited more efficiently. When externally grounded, the gold pads also reduces the direct RF coupling between the top plate electrode and the transducers. This shielding effect helps in reducing the spurious signal level of the device.

A zinc oxide layer 1.6 μm thick is then RF-sputtered on the substrate to provide the piezoelectric coupling between the acoustic surface wave and the diode array. The RF sputtering system used has been described by Khuri-Yakub, et al.[4] The important deposition parameters are shown in Table 1.

Table 1. RF Sputtering Conditions

Substrate Temperature	250°C ± 1°C
RF Input power	160 Watts
Sputtering atmosphere	80:20, Argon:Oxygen
Deposition pressure	8 microns
Deposition rate	180 - 200 Å/min

The transducers and the top electrode are fabricated using the standard lift-off of positive photo resist. Gold wires are bonded to the devices with silver epoxy. This compression-free bonding technique gives more consistent results than the conventional thermal compression technique.

III. Performance of the ZnO-on-Si Storage Correlator

The interdigital transducers on our device are 10 finger pairs. Simple inductance tuning gives a 7 MHz bandwidth with a center frequency of 125 MHz. The terminal-to-terminal insertion loss is approximately 17 dB. The length of the active diode array is 3 μsec. When operated as a convolver, this device gives an overall convolution efficiency of -64 dBm, which is comparable to that obtained with the air-gap devices.

One of the problems encountered in assembling the air-gap devices is to maintain a uniform airgap along the length of the diode array so that the electric field couples uniformly to each individual diode. Since the monolithic storage correlator does not have an air gap, this particular problem is eliminated from the fabrication process. Highly uniform zinc oxide film can usually be obtained over large areas under tightly controlled deposition conditions. This implies that high performance devices can be batch-fabricated, thus making it compatible with the integrated circuit technology. The uniformity of the ZnO film can best be demonstrated by storing a uniform charge into the diode array and then reading it out by applying a short RF pulse to the top electrode. Figure 2 is the output signal obtained with a 25 ns readout pulse using this technique. It is seen that the interaction is uniform to within 1 dB along the whole 3 μsec length of the diode array.

It is interesting to note that the diode array can also be envisioned as an array of MOS transistors with each individual diode acting as either the source or the drain of a MOS transistor. Therefore, the surface potential of the n regions between diodes can be controlled by DC bias applied to the top plate electrode. With negative bias, inversion layers start to form between diodes and form a shunting layer between the diodes and thus causing the storage output to drop very quickly. With positive bias, electrons moving to the surface will eventually form an accumulation layer. The storage output in this case also drops, probably due to the fact that the accumulation layer provides a

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shunting path for the signals applied to the top plate electrode. For most, but not all of the devices we have made, positive DC bias is needed to obtain the optimal surface potential for storage. In contrast to the air-gap device, the biasing voltage involved is only a few volts. This is just one example to support the argument that unlike the air-gap device, the monolithic storage correlator is a much easier type to interface with other electronic systems.

For fixed writing (P_W) and reading (P_R) signal levels, the input dynamic range of the storage correlator is defined as the range over which the correlation output power varies linearly with that of the signal to be stored (P_S). The various power levels used are shown in Fig. 3. For the air-gap correlators, the minimum detectable signal is limited by the spurious bulk-wave generation by the readout signal, due to the high RF fields applied across the thick piezoelectric substrate. Therefore, instead of having its full dynamic range available (60 dB or more), the dynamic range is only 25 - 35 dB at the present time. The elimination of these spurious signals in air-gap devices appears to be very difficult, if not impossible. For the ZnO-on-Si storage correlator, since the piezoelectric ZnO film is only 1.6 μm thick (0.05 λ), spurious bulk wave generation is not a problem.

Other sources of spurious signals do exist and our present effort is concentrated on reducing them. The most obvious of these is the direct RF pickup by the output transducers. By careful design of the enclosing metal box and solid grounding of the back side of the device, we have reduced this direct pick-up below the thermal noise level of the measuring system. The metal box is partitioned into three cavities for matching networks and each cavity can be tightly closed by separate covers. The grounding of the device is accomplished by soldering the back side of the sample using indium solder to a small carrier box with lead wires connected to the proper matching networks. The ends of the top plate electrode represent sharp terminations of the electric field applied to the ZnO film and give rise to spurious surface wave generation. This can easily be eliminated by slanting the two ends of the electrodes, leaving a background spurious signal level of about -70 dBm. This gives an input dynamic range of 30 - 40 dB. Though the study of the nature of this spurious signal is not completed yet, we do know that it is due to surface wave generation and it can be affected by DC bias applied to the top plate electrode. This DC bias effect suggests that it is one associated with the silicon surface. For historical reasons, we have been using a staggered diode array structure which introduces unwanted spatial periodicities. The frequency spectrum of the feedthrough tends to confirm this conclusion. Therefore we are currently making more devices using a simpler array structure, which we hope will eliminate the residual feedthrough.

IV. Signal Processing Using the Input Correlation Technique[2,5,6,7]

A number of authors have previously described the operation of the storage correlator as an analog signal processor. Here, we wish to describe our experiments with the ZnO-on-Si correlator using the so-called input correlation technique. The simplest example of this mode of operation is illustrated schematically in Fig. 4(a), where two identical linear FM chirps with chirp slope μ have been correlated during the write-in process. The top plate chirp is a delayed replica of the acoustic chirp so that at only near one point of the diode array, the frequencies of the top plate chirp will match those of the acoustic chirp fed into port A during the complete length of these chirps. By properly choosing the power levels of the signals, successive charging of the diodes due to the entire chirps will store a charge spike near this point corresponding to the correlation peak of the two signals. This correlation peak can be readout directly at port B later by applying a short pulse to the top plate. Figure 5 shows the direct correlation output of two 40 μsec, 6 MHz linear FM chirps. It is important to note that with this mode of operation, the time bandwidth product of the signals that can be processed is now limited by the bandwidth of the acoustic transducers and the storage time of the diode array, not just the acoustic delay of the diode array. Since the storage time of the diode array can be as much as several hundred milliseconds or more, this can conceivably lead to correlation TB products larger than 10^6.

The spectral resolution of this technique is demonstrated by the experiment schematically shown in Fig. 4(b). One of the linear FM chirps of frequency $\omega = \omega_1 + \mu t$ is AM modulated by a sinusoidal wave form of frequency ω_m and applied to the top plate electrode. The resultant signal can be regarded as the superposition of three chirps of frequencies $\omega = \omega_1 + \mu t$, and $\omega = \omega_1 + \mu t \pm \omega_m$. Since the frequencies of the three chirps will match that of the acoustic chirp at different positions along the diode array, three correlation peaks will be stored, corresponding to the carrier frequency and the two sidebands introduced by the AM modulation. The bottom trace of Fig. 6 shows the output signal obtained by using a short RF pulse (100 ns) to readout the stored correlation peaks. The chirps used are 5 ms long with a bandwidth of 6 MHz, corresponding to a TB product of 3×10^4. Since the carrier has been suppressed, the two correlation peaks correspond to the two sidebands. The frequency of the AM modulation used is 186 Hz, indicating that the frequency resolving power of the device is about 372 Hz for this particular case. By varying the chirp lengths, frequency components in different frequency ranges can be observed. The top trace is the output signal when the short readout pulse alone is applied to the device, thus representing the spurious signal levels of the device.

In order to readout the stored correlation peaks accurately, the readout pulse used in Fig. 4(a) has to be sufficiently short. This is because the information corresponding to the correlation peak is stored only in a narrow region of the silicon diode array corresponding to a few diodes. Therefore, on readout, the output signal obtained is relatively weak and has a limited dynamic range. This situation can be improved by using the technique shown in Fig. 4(c), where the chirp slope of the signal fed into the center terminal is changed to μ_2 to differ slightly with the acoustic chirp slope μ_1. In this case, the frequencies of the two chirps will be identical at one end of the diode array at the beginning of the chirps, and at the other end of the diode array at the end of the chirps. In this way, the original long chirp has been compressed as a stored charge pattern into a short chirp during the write-in process. By choosing $(\mu_1 - \mu_2)/\mu_1 = T_A/T_C$, where T_A is the acoustic wave delay of the diode array and T_C is the length of the chirp, the compressed chirp will occupy the whole length of the diode array. The storage process is thus similar to holographic storage and a pulse compression technique similar to holographic reconstruction can be employed on readout. A chirp of time length T_A with a slope of $\mu_1^2/(\mu_1 - \mu_2)$ is used to readout the signal, and a far larger signal than with the simpler process already described can be obtained. The theoretical improvement in signal-to-noise ratio to be expected is approximately BT_A, where $B = \mu_1 T_C/2\pi$ is the bandwidth of the chirps. Figure 7 shows the correlation peak of two 2 ms, 6 MHz bandwidth

linear FM chirps obtained with this two-step compression technique. The compression ratio is about 8000. The S/N ratio of this output is approximately 13 dB higher than the case using two identical chirps, which is close to what would be expected theoretically. The side lobe levels could be reduced by eliminating the spurious signals in the device and by using more linear FM chirps.

V. Conclusion

We conclude that an efficient monolithic ZnO-on-Si storage correlator can be fabricated. Due to the monolithic nature of the device, its fabrication technology is compatible with the standard IC technologies. So far, the performance of this device is close to what we would expect from such a structure. By reducing the spurious signal levels furthermore, which we believe is less difficult than on the air-gap devices, this monolithic device may become a practical signal processor offering large dynamic ranges. The input correlation experiments have demonstrated that it offers the possibility of correlating signals with extremely large time bandwidth products determined by the storage time of the diode array and the bandwidth of the transducers.

Acknowledgement

The authors wish to thank L. Goddard for his work on the ZnO deposition.

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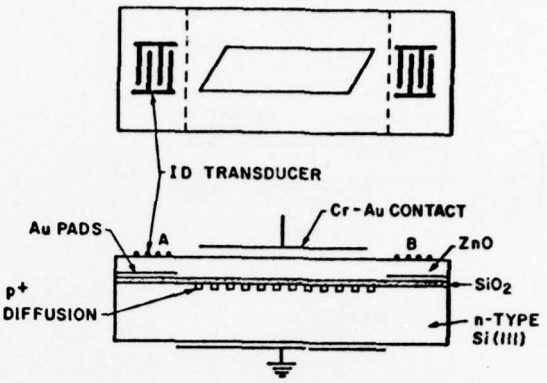

FIG. 1--Schematic of zinc-oxide-on-silicon monolithic storage correlator.

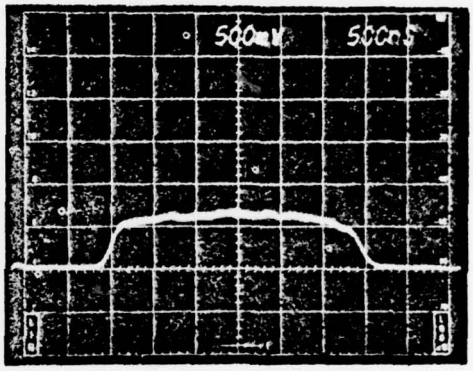

FIG. 2--ZnO-on-Si storage correlator interaction region uniformity.

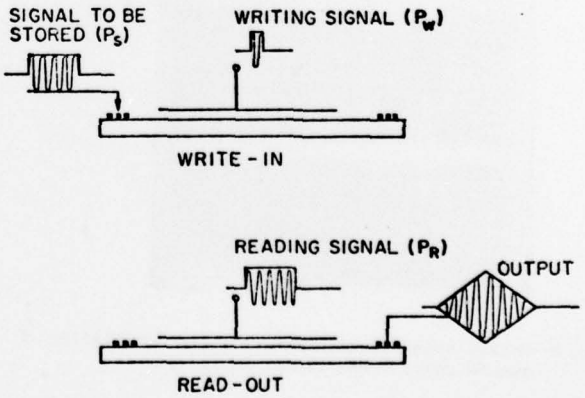

FIG. 3--Write-in and readout of the storage correlator.

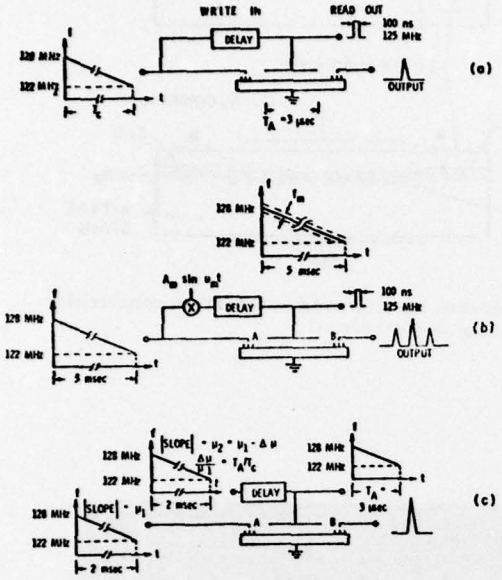

FIG. 4--(a) Direct input correlation;
(b) Spectral resolution of input correlation;
(c) Two-step compression technique.

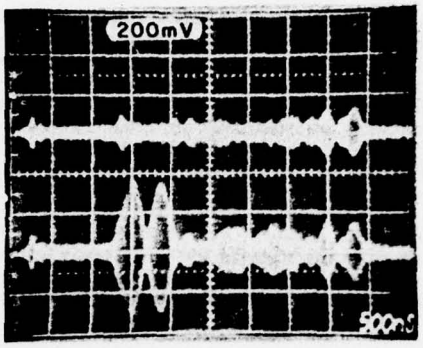

FIG. 6--Correlation output of the AM modulation experiment.

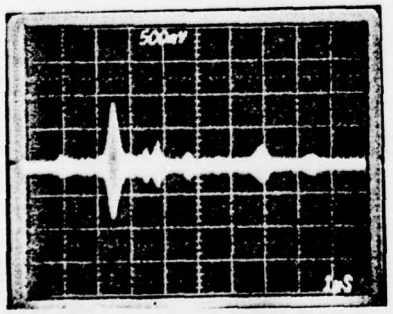

FIG. 5--Output obtained with direct input correlation of two 40 μsec, 6 MHz linear FM chirps.

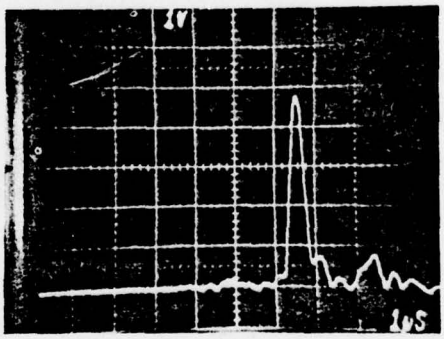

FIG. 7--Correlation output of two 2 msec, 6 MHz linear FM chirps using the two-step compression technique.

INPUT CORRELATION WITH THE A.S.W. STORAGE CORRELATOR

Indexing terms: Acoustic-surface-wave devices, Correlators

By correlating during read-in, we correlate signals of much greater length than could be stored within the device, thereby obtaining a large improvement in t.b. product.

The acoustic-surface-wave storage (or memory) correlator has recently received considerable attention as a high-bandwidth signal processor.[1] We consider here a new mode of device operation that affords greatly increased time–bandwidth product, namely input correlation.

The device consists of a p–n-junction-diode array situated above a piezoelectric surface-wave delay line. Fig. 1*a* shows a typical mode of operation whereby the modulation $W(t)$ of a signal $W(t)e^{j\omega t}$ is written into the diode array as a stored charge pattern and read out at some later time as a correlation with a reading signal $R(t)e^{j\omega t}$.

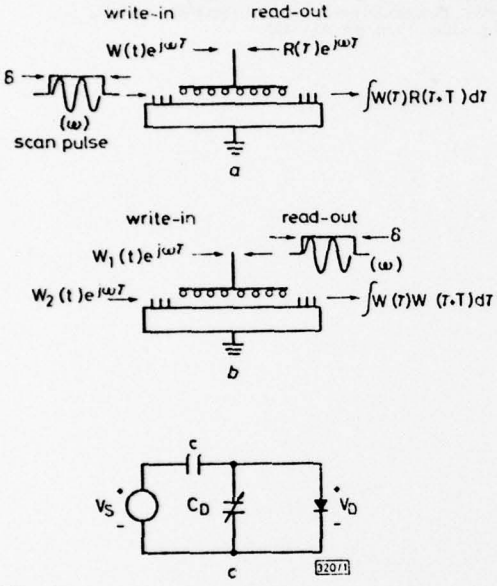

Fig. 1
(*a*) A typical mode for storage and output correlation
(*b*) Input correlation and readout
(*c*) Equivalent-circuit model

The writing process involves the interaction of two r.f. inputs. We consider first the case where one is used to excite a short acoustic-surface-wave pulse and the other is applied to the diode array through a capacitor, the capacity between the diode array and the ground electrode on the other side of the delay line. Thus the source in Fig. 1*c* is of the form $V_s = Se^{j(\omega t - kz)} + W(t)e^{j\omega t}$, where S is a constant. The surface-wave term is assumed to be dominant, but still of insufficient strength to allow the diode conduction current to exceed its displacement current. Thus the voltage divider consisting of C and the diode depletion-layer capacitor C_D determines the diode voltage V_D. During successive peaks of the surface-wave potential, small amounts of forward diode current flow. This puts successive increments of charge into the capacitor C, owing to both S and $W(t)$.

After the surface-wave pulse passes by the diode, $V_s \simeq 0$, so that the capacitor C is placed across the diode, reverse biasing it. The stored charge now leaks out slowly through the diode reverse current. The reverse-biased diode acts like a varactor whose capacity depends on the stored charge. A readout signal $R(t)e^{j\omega t}$ applied to the diode array excites a surface wave whose amplitude depends on the diode capacities. This wave appears at the transducer opposite the one used for input as the correlation of R and the stored-charge pattern.

By solving the p^+–n-diode diffusion equation for times much shorter than the minority-carrier recombination time, we can show that the diode neutral-region charge increases logarithmically in time during the charging process as[4]

$$Q(t) = \frac{kT}{q} C_D \ln\left[1 + \frac{q^2 p_{n0} t}{\pi k T C_D}\left(\frac{\omega D_p kT}{3\pi qS}\frac{C+C_D}{C}\right)^{\frac{1}{2}} \times \exp\left(\frac{qS}{kT}\frac{C}{C+C_D}\right)\right]$$

where S is the peak surface-wave potential,

$$C_D = \sqrt{\frac{2qN_D C_s}{V_B - V_D}}$$

is taken at the peak value of V_D, p_{n0} is the thermal-equilibrium minority-carrier concentration, D_p is the minority-carrier diffusion constant, N_D is the doping density and ω is the frequency.

Since $V_D(z, t)$ has some direct component V_0, a pure r.f. component $W(t)e^{j\omega t}$ and a component due to the surface wave $S(z, t)e^{j(\omega t - kz)}$, expansion of the above equation yields a product term of the form $WSe^{jkz}\ln(Bt)$, where B is a constant. The logarithmic characteristic allows charge to be integrated over long intervals by appropriate choice of the input levels. Because this component of charge varies with the product of the two input signals, it is also possible to correlate two long signals during the charging process. At present, unless S is carefully chosen so as to use only a linear portion of the charging characteristics, the nonlinear time dependence makes this technique poorly suited for amplitude-dependent correlations. It would, nevertheless, be of considerable use in phase-sensitive correlations, such as those performed with f.m. chirps. Modifications can, however, be performed to charge linearly from a current source, as described by Ingebrigtsen.[3]

The t.b. product is normally limited by the transducer bandwidth and diode array length. Input correlation allows correlation of signals much longer than could normally be stored, yielding a corresponding increase in t.b. product. For example, the longest convolver so far constructed covers a 35 μs signal in its 12·1 cm length.[4] By careful adjustment of signal levels, input correlation should allow correlation of signals $\gtrsim$1 ms long, yielding a t.b. improvement of at least

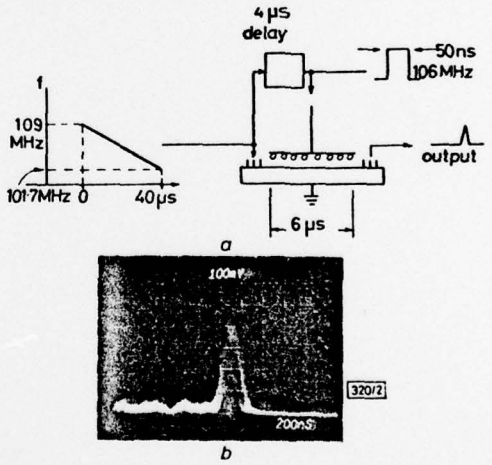

Fig. 2
(*a*) Input-correlation experimental set-up
(*b*) Correlation output

30, and, in certain applications, obviating the need for a long diode array.

We have experimentally demonstrated this by input correlating two linear f.m. chirps. Fig. 2*a* shows the experimental set-up. The plate chirp is a delayed replica of the acoustic chirp, so that the plate and surface-wave frequencies will match near one point along the diode array. A correlation peak will be stored there, which may be directly read out at some later time.

Our device had a centre frequency of 105·5 MHz and a 3 dB bandwidth of about 7 MHz. The mesa p^+–n-diode array length was 2 cm (6 μs). The acoustic and plate inputs were both 40 μs, 7·3 MHz linear f.m. chirps with a centre frequency of 105·4 MHz. To obtain the plate delay, a common chirp

was generated and mixed up in frequency before being applied after a 60 μs delay. Both plate signal amplitudes were 8 V zero to peak. The acoustic signal was 23·5 dBm and the minimum 2-port delay-line loss was 18·5 dB at 106 MHz.

The correlation output is seen in Fig. 2*b*. The width at half maximum is 180 ns, corresponding to a compression ratio over the original 40 μs inputs of 220. The theoretical compression, corresponding to the t.b. product, is

$$40\ \mu s \times 7{\cdot}3\ MHz = 292.$$

It should be noted that the observed output is actually the correlation of the 50 ns read-out pulse with the stored-charge pattern, thus broadening the output about 10% over the true correlation charge pattern. Nevertheless, the performance improvement is dramatic. In the output correlation mode, the peak compression obtainable is limited by the diode array length and transducer bandwidth to about

$$6\ \mu s \times 7{\cdot}3\ MHz = 44,$$

or about 20% of that obtained through input correlation.

Thus, input correlation removes the t.b. limit imposed by the finite diode array length. The technology required to correlate certain extremely long signals then becomes far simpler, allowing extremely high t.b. signal processing with the storage correlator.

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30th June 1977

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APPENDIX E

The charging process in the acoustic surface wave *p-n* diode storage correlator[a)]

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We demonstrate analytically and experimentally that the acoustic surface wave *p-n* diode storage correlator may be charged either very quickly or very slowly, depending on the input signal levels, and independent of the diode storage time. Thus, the same long storage time device is usable for both high-speed and slow (such as integrating) applications.

PACS numbers: 43.60.Qv, 43.35.Yb, 72.50.+b, 85.30.De

Storage correlators employing both Schottky[1] and *p-n*[2,3] diodes have been demonstrated. The relationship between the charging and storage processes has not been well understood, and it has been generally assumed that devices exhibiting long storage times will require long charging times. We have theoretically and experimentally demonstrated that this is not so.[1] Charging time depends mainly on the input levels; thus, even long storage time *p-n* diodes may be charged during periods adjustable from 1 nsec to 1 sec or longer.

The storage correlator configuration is shown in Fig. 1(a), with corresponding equivalent circuits in Figs. 1(b) and 1(c). An array of *p-n* diodes fabricated on a semiconductor interacts with a surface wave traveling on a neighboring substrate. In the charging process, a short pulse applied to the diode array switches each diode on. The capacitor charges up to a voltage corresponding to that of the pulse [Fig. 1(b)]. When the pulse amplitude drops to zero, the capacitor remains charged and the diode becomes reverse biased, so that stored charge is slowly lost through the diode leakage current. In actual operation, the diode voltage is the sum of two terms, one due to the acoustic surface wave and the other due to the pulse. After charging, the reverse-biased diodes act like varactors, their capacities depending on the stored charge. If a later signal is applied to the array, it will excite a potential on the piezoelectric substrate whose amplitude depends on the diode capacities. By this means, the stored charge may be read out.

In another paper, we present a complete theory of this operation. Here we only discuss the diode charging and show that, although *p-n* diodes are reputed to be slow, it is indeed possible to read signals into these

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diodes in nanosecond intervals, independent of the storage time. Furthermore, by employing smaller potentials, it is possible to charge relatively slowly in an integrating mode.

To understand the charging process, we consider the action of switching on the diode by accounting for its transient response. To do this, we first consider the case of charging with a single short pulse [Fig. 1(b)]. By solving the p^+-n junction diffusion equation for times much shorter than the hole recombination time, we can show that the diode voltage V_D is

$$V_D(t)=\frac{kT}{q}\ln\left(1+\frac{1}{p_{n0}(\pi D_p)^{1/2}}\int_0^t\frac{J(\tau)}{(t-\tau)^{1/2}}\,d\tau\right), \tag{1}$$

where the current density at a time τ is $J(\tau)=-qD_p(\partial p/\partial x)$ and $p(x=0,t)=p_{n0}[\exp(qV_D/kT)-1]$. D_p is the diffusion constant for holes, q the electronic charge, and p_{n0} the minority carrier density in the n layer in thermal equilibrium. We assume that the diode is charged through a capacitor C with a pulse of the form $V(t)=V_0\times[1-(t-t_0)^2/t_0^2]$, as in Fig. 1(b). Then if the conduction current through the diode is much larger than the displacement current, the current varies linearly in time. It follows from Eq. (1) that the diode voltage is

$$V_D(t)=\frac{kT}{q}\ln\left[1+\frac{4CV_0t^{1/2}}{qp_{n0}t_0(\pi D_P)^{1/2}}\left(1-\frac{3t}{2t_0}\right)\right]. \tag{2}$$

At $t=\frac{3}{2}t_0$, when $V=\frac{3}{4}V_0$, the diode becomes reverse biased, and, hence, three-fourths of the peak charge in the capacitor C is stored. Successive pulses will asymptotically increase the stored charge to the maximum value CV_0.

A second case is when relatively weak signals are used to charge the diodes. Now the capacitive current of the diode dominates and the circuit model of Fig. 1(c) is appropriate. Here we solve the diffusion equation for a sinusoidal voltage excitation to find the diode current. The charge in the capacitor, due to this current, increases logarithmically in time as

$$Q(t)=\frac{kT}{q}C_D\ln\left[1+\frac{q^2p_{n0}t}{\pi kTC_D}\exp\{qV_0[C(C+C_D)]\}\times\left(\frac{kT\omega D_p}{3qV_0}\frac{C+C_D}{C}\right)^{1/2}\right], \tag{3}$$

where ω is the frequency and $C_D=[2qN_D\epsilon_S/(V_B-V_D)]^{1/2}$ is the diode capacitance, taken to be constant, V_B is the built-in diode voltage, and V_D is taken at its maximum value in defining the capacitance.

In an actual device, the stored charge pattern results from the read in of a small rf signal $\varphi_a\exp(j\omega t)$ on a transducer and a signal $\varphi_p\exp(j\omega t)$ on the plate. Assuming that the dominant potential at the diode is due to φ_p, it is as if the applied potential V_A is of the form

$$V_A=A\varphi_p+(B\varphi_a)\exp(-j\omega x/v), \tag{4}$$

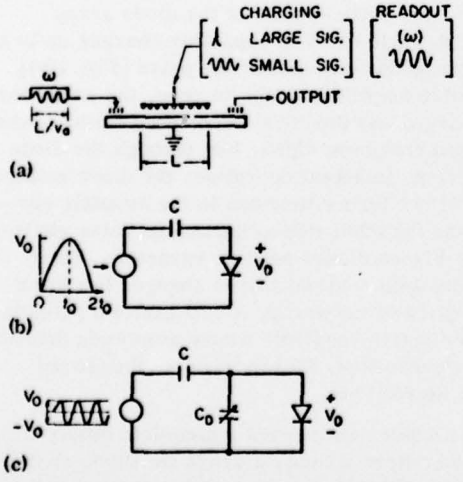

FIG. 1. (a) Storage correlator configuration and operation. (b) Charging model for a single large pulse. (c) Charging model for a small signal.

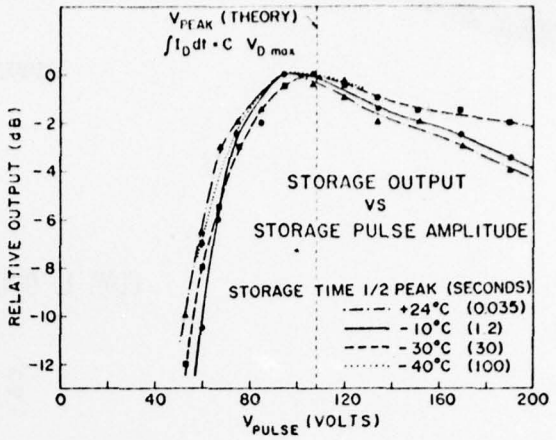

FIG. 2. Correlation output as a function of the amplitude of the charging pulse over a 64 °C temperature range.

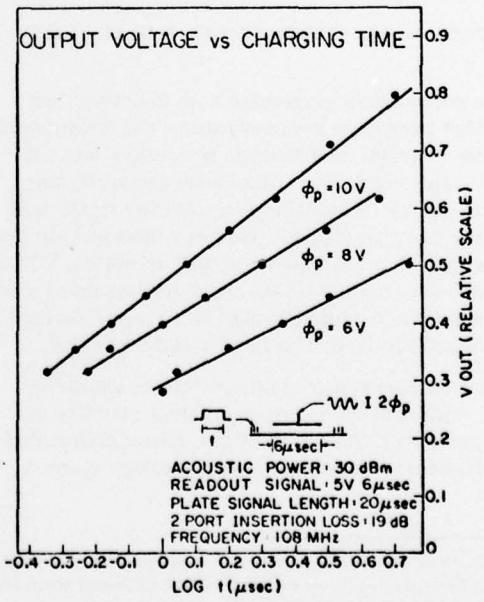

FIG. 3. Correlation output as a function of the charging time and rf input voltage φ_p.

where A and B are constants, v is the acoustic velocity, and x is the position of the diode.

Inserting this result in Eq. (3), we can show that there will be a stored component of charge with a spatial wave number $k = \omega/v$, which varies as $\varphi_p \ln(Kt)$ where K is a constant.

The significant results of this anslysis are twofold:

(1) The diodes can be charged to 75% of the maximum value with a single pulse of sufficient amplitude and duration less than one-half the rf cycle.

(2) For small amplitude pulses, the stored charge varies logarithmically with time. Thus, the charging rate can be very low.

We have performed experiments to verify these results. The device employed a mesa p-n diode array[5] with a room-temperature storage time of 35 msec. The frequency was 108 MHz and the charging pulse length was ~5 nsec. While the storage time varied by more than three orders of magnitude, the charging characteristics remained almost constant over a 64 °C temperature range as shown in Fig. 2. This is expected from Eq. (2) since $n_i \propto T^{3/2} \exp(E_g/2kT)$ and V_D is virtually independent of T. This proves that a very long storage time diode can be charged with a very short pulse of sufficient amplitude.

The same device can also exhibit slow charging characteristics under the proper conditions, i.e., with small amplitude charging signals. In Fig. 3 a plot of the device output is given as a function of the logarithm of the charging time. The output and output slope both vary as $\varphi_p \ln t$, as predicted in the discussion following Eq. (3).

The logarithmic charging behavior has been observed in earlier experiments.[2,6] Such observations were interpreted to show that long storage time diodes will exhibit slow charging characteristics. The present work indicates that those results were due to the low levels of the charging signals, and not to any inherent physical limitations of the diodes.

To conclude, through the proper choice of input signal levels, the charging time may be varied from a few nanoseconds or less to 1 sec or more. Furthermore, this behavior will be independent of the diode storage time.

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A monolithic zinc-oxide–on–silicon *p-n*-diode storage correlator[a)]

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A monolithic zinc-oxide–on–silicon *p-n* storage correlator has been constructed. When operated both as a convolver and as a storage correlator, the electronic efficiency obtained with this device is comparable to that of the present $LiNbO_3$ airgap devices. This device has the potential of having very large dynamic range because of the absence of spurious bulk-wave generation, as occurs in the airgap device. Several signal-processing functions have been demonstrated with this new type of storage correlator. In one chirp correlation experiment, correlation of signals with a time-bandwith product of 4000 has been observed.

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Because of its wide applications as a signal-processing device, the storage correlator has attracted much attention in the past two years.[1–3] All the storage correlators with diode arrays that have been fabricated so far are of the so-called airgap type, where a substrate of silicon with diode array on it is separated by an airgap from a $LiNbO_3$ delay line. In order to achieve efficient and uniform interaction between the acoustic wave and the diode array, sophisticated assembly techniques have to be used to maintain a thin airgap typically of the order of 2000 Å along the whole length of the diode array. This requires that each device be assembled and adjusted individually. For this reason and others to be explained latter, a monolithic structure is desirable.

In this paper we describe such a monolithic storage correlator. The configuration of the device is schematically shown in Fig. 1. This configuration is very similar to that of the zinc-oxide—on—silicon convolver demonstrated by Khuri-Yakub and Kino.[4] A zinc-oxide layer 1.6 μm thick is rf sputtered on the Si substrate to provide the piezoelectric coupling between the acoustic surface wave and the silicon. The rf power used for the deposition is 160 W and the Si substrate is kept at 250 °C throughout the sputtering process. The oriented gold pads at each end of the delay line provide slightly better underlayers than SiO_2 for the zinc-oxide growth. These pads also act as ground planes for the interdigital transducers which are deposited on top of the ZnO layer on the gold pads. The 10-finger interdigital transducer is designed to launch a 1-mm-wide acoustic beam at 125 MHz center frequency. The *n*-type (111) Si substrate used has a resistivity of 9—15 Ω cm. The p^+-*n* diodes on the surface of the Si substrate are 4 μm wide with a 4-μm spacing between diodes. These diodes are fabricated by shallow boron diffusion (≈0.6 μm) following a n^+ gettering phosphorus diffusion on the back of the Si wafer. This gettering process reduces the number of metallic ions present at the Si surface; thus diodes with low leakage current can be fabricated reproducibly.

Simple inductance tunning for the two transducers yields a terminal-to-terminal loss of about 19 dB with a 3-dB bandwidth of 8 MHz. When used as a convolver, this device gives an overall convolution efficiency of −66 dBm. Considering the fact that the diodes occupy only half the area of the active silicon region, this number compares favorably with −58 dBm as predicted and measured by Khuri-Yakub and Kino[4] for their zinc-oxide convolvers.

Several modes of operation are possible when this device is used as a storage correlator. In the present case, the writing process is accomplished by storing a charge pattern in the diode array through the simultaneous presence of an rf signal applied to the top plate and the electric fields associated with the acoustic signal launched by transducer A. After the storage interval, by applying another rf signal to the top plate, the correlation of this signal with the stored signal is obtained at the acoustic port B. In this mode of operation we have observed a 65-dB output dynamic range with a 3-dB storage time of 20 msec or more, with the maximum acoustic input level of 26 dBm at the acoustic port and 6 V *p-p* at the input terminal of the top plate both for write-in and read-out.

It is important to note that due to the presence of the rf signal on the top plate during read-out, spurious signals will be detected along with the correlation output. These spurious outputs are caused either by direct rf pick-up by the output port or by the surface-wave and/or bulk-wave generation when the piezoelectric

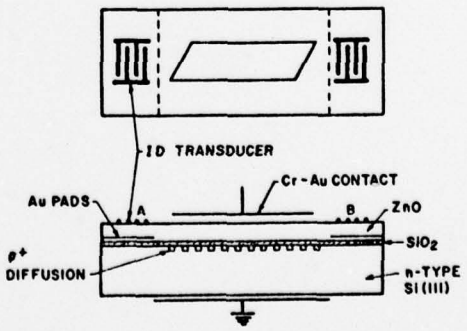

FIG. 1. Schematic of the zinc-oxide—on—silicon monolithic storage correlator.

a)Work supported by the Office of Naval Research under contract N00014-76-C-0129.

zinc-oxide film is excited by the top-plate rf signal. The direct rf feedthrough has been reduced below the thermal noise of the measuring system by extremely careful design of the enclosing metal box and by properly grounding the silicon substrate.

Since the piezoelectric zinc-oxide film on our device is only 1.6 μm thick, bulk-wave generation by the read-out signal which severely limits the input dynamic range of the airgap storage correlator is not present; this is a major advantage. Therefore, our main concern is with spurious surface-wave generation either from the ends of the top plate or from the whole length of the active zinc-oxide film underneath the top plate. By slanting the ends of the top plate; the former effect has been eliminated. The spurious surface-wave generation by the whole active region underneath the top plate at the present time limits the input dynamic range of our device to 30—35 dB; i.e., the range over which the level of the signal to be stored can be varied during the write-in process before the correlation output drops to the spurious signal level.

Our present hypothesis for the cause of this spurious signal is that the diode array perturbs the surface waves. Therefore, any structural periodicity appearing in the diode array which matches the wavelength of the rf signals used can cause surface-wave generation. In support of this argument, we note that the level of the spurious signal can be affected by dc bias applied to the top plate which controls the surface potential of the n-type regions between diodes. Effort is under way at the present time to fabricate new devices with a simplified array structure. Unfortunately, for historical reasons, the present diode elements are staggered giving an additional periodicity of 130 μm, which could cause the unwanted spurious surface-wave generation through its fourth harmonics.

Several signal-processing functions have been demonstrated with this device. Figure 2 shows the storage correlation of a 5-bit Barker code. The Barker code is stored in the diode array by feeding it to the top plate and at the same time passing a 200-nsec acoustic pulse underneath it. The side lobe level is within 2 dB of the theoretical value of −14 dB. A second experiment demonstrates that integration and correlation between two input signals can be obtained. Two identical linear FM chirps are inserted simultaneously into both the

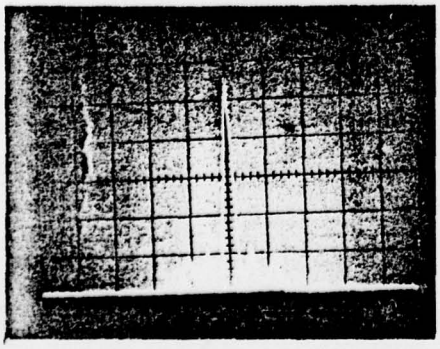

FIG. 2. Storage correlation of a 5-bit Barker code. (Horizontal: 2 μsec/div.)

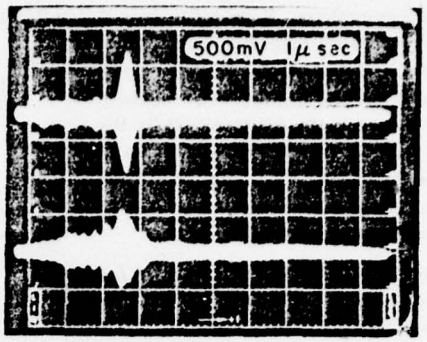

FIG. 3. Correlation peak obtained with (a) 700-μsec 6-MHz (b) 350-μsec 3-MHz linear FM chirps.

acoustic port and the top plate.[5-7] These signals are arranged to be of low enough level so that many rf cycles are required to saturate the diodes. In this case the device stores a component of charge which is proportional to the integral of the product of the two signals, i.e., if the signals are $F(t)\exp(j\omega t)$ and $G(t)\exp(j\omega t)$, respectively, the stored signal is

$$H(x)=\alpha\int F(t-x/v)\,G(t)\cos(\omega x/v)\,dt,$$

where α is a constant and v is the acoustic-wave velocity. By delaying one chirp by 3 μsec with respect to the other we obtain the stored correlation peak of the two chirps in a short region along the diode array. Thus the long chirp is compressed into a narrow charge spike stored in the diode array. The compression ratio depends on the time-bandwidth product of the chirp used which in turn is only limited by the bandwidth and storage time of the device. Since the storage time of the device can be very long (a few hundred msec or more), extremely large compression ratios can be achieved.

Trace (a) of Fig. 3 shows the correlation output obtained with a short pulsed read-out signal of approximately 100 nsec. It will be observed that the output is 200 nsec wide, when the input FM chirp is 700 μsec long and has a frequency excursion of 6 MHz. This represents a compression ratio of about 3500. As a check on this result, we note with trace (b) that when the chirp is gated to 350 μsec long, thus reducing the bandwidth by a factor of 2, the compressed output pulse widens by a factor of 2, and its amplitude drops; in addition the sidelobe levels become much worse—probably due to the fact that this device is as yet not a true linear integrator. As demonstrated by Ingebrigtsen and Stern[8] we believe that it should be possible to operate the device in a linear integration mode. These experiments demonstrate that like the airgap storage correlator, this monolithic device stores both the amplitude and phase of a signal and demonstrates that correlation of extremely large time-bandwidth product signals can be obtained.

We conclude that an efficient monolithic zinc-oxide—on—silicon storage correlator can be fabricated. Its capability and versatility as a signal-processing device have been demonstrated. Because of the absence of

spurious bulk-wave generation, it may become a practical signal-processing device offering large dynamic ranges, both at input and at output. In addition it offers the possibility of correlating signals with extremely large time-bandwidth products determined by the storage time of the device and the bandwidth of the transducers. As storage times can be 1 sec or more and bandwidth in the tens of MHz range, the possible signal-processing capability is impressive.

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